Max FIFO
Application Note

Application Note – Max FIFO

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1. Introduction

BMI270 is an ultra-low power IMU optimized for wearable applications. The IMU combines precise acceleration and angular rate measurement with intelligent on-chip motion-triggered interrupt features. The 6-axis sensor combines a 16-bit triaxial gyroscope and a 16-bit triaxial accelerometer in a compact 2.5 x 3.0 x 0.8 mm3 LGA package

BMI270 is a member of Bosch Sensortec's BMI260 family of IMUs, targeting fast and accurate inertial sensing in wearable applications. BMI270 features Bosch's automotive-proven gyroscope technology with an improved accelerometer. Significant improvements in BMI270 include, but are not restricted to, the overall accelerometer performance, i.e. an extremely low zero-*g* offset and sensitivity error, low temperature drifts, robustness over PCB strain and a low noise density.

BMI270 features the industry's first self-calibrating gyroscope using motionless CRT (Component Re-Trimming) functionality to compensate MEMS typical soldering drifts, ensuring post-soldering sensitivity errors down to ± 0.4%.

BMI270 includes intuitive gesture, context and activity recognition with an integrated plug-and-play step counter/detector, which is optimized for accurate step counting in wrist-worn devices. The IMU is also well suited for other types of wearable devices, such as hearables, smart clothes, smart shoes, smart glasses and ankle bands.

BMI270 is available in application-specific versions: gesture and context & activity. The 'gesture' version includes flick in/out, arm up/down, and wrist tilt features. The 'context and activity' version has advanced features for recognizing context activity and activity change, for example standing, walking and log car parking by detecting the activity change.

In case none of the features are needed but FIFO size is critical, there is a Max FIFO configuration.

1.1. Max FIFO

This application note describes the Maximum FIFO configuration of BMI270 that offers 6 KB of FIFO. Users benefit from system-level power savings as the host (µC) does not need to be awake all the time.

For complete details regarding BMI270 specifications (e.g. pin-out, power modes, self-test, temperature sensor, Sensor Time, FIFO), Digital interfaces (primary/secondary), landing pattern, HSMI and sensor API refer the following:

https://www.bosch-sensortec.com/products/motion-sensors/imus/bmi270.html

https://www.bosch-sensortec.com/media/boschsensortec/downloads/datasheets/bst-bmi270-ds000.pdf

https://github.com/BoschSensortec/BMI270-Sensor-API

2. Quick Start Guide

The purpose of this section is to help developers who want to start working with BMI270 by giving some basic hands-on application examples to get started.

2.1. Note about using BMI270

The communication between application processor and BMI270 will happen either over I2C or SPI interface.

Each register read operation includes dummy bytes:

- I2C: 0
- SPI: 1

For simplicity the dummy bytes are not shown in the examples below.

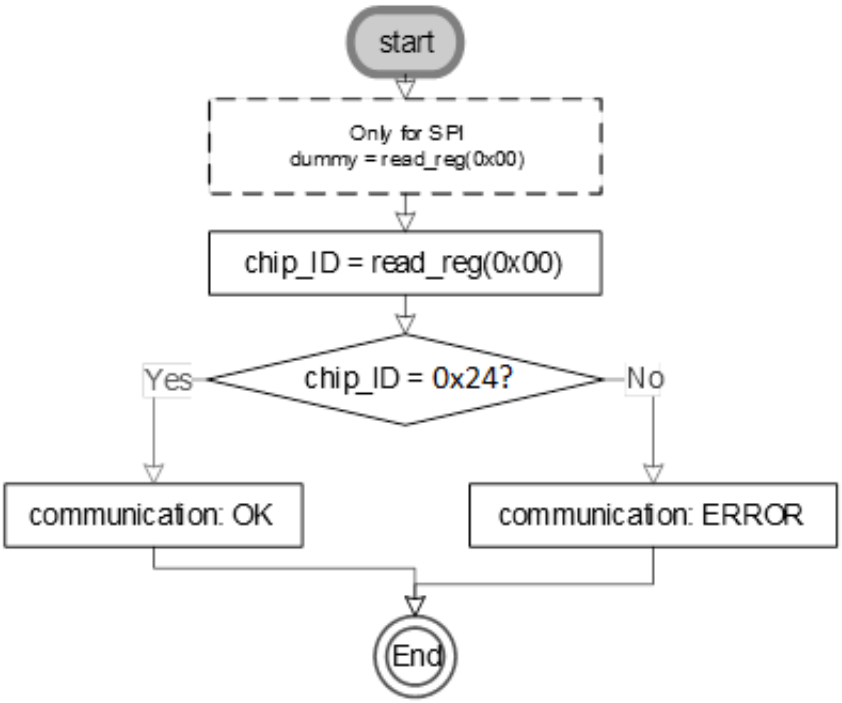
Before starting the test, BMI270 has to be properly connected to the master (AP) and powered up. The device is configured for advance power save mode after POR or soft reset. For details on the interface operation in advanced power save mode, see the description of Register PWR_CONF.adv_power_save For more information about the interfaces, see BMI270 data sheet

2.2. First application setup examples algorithms:

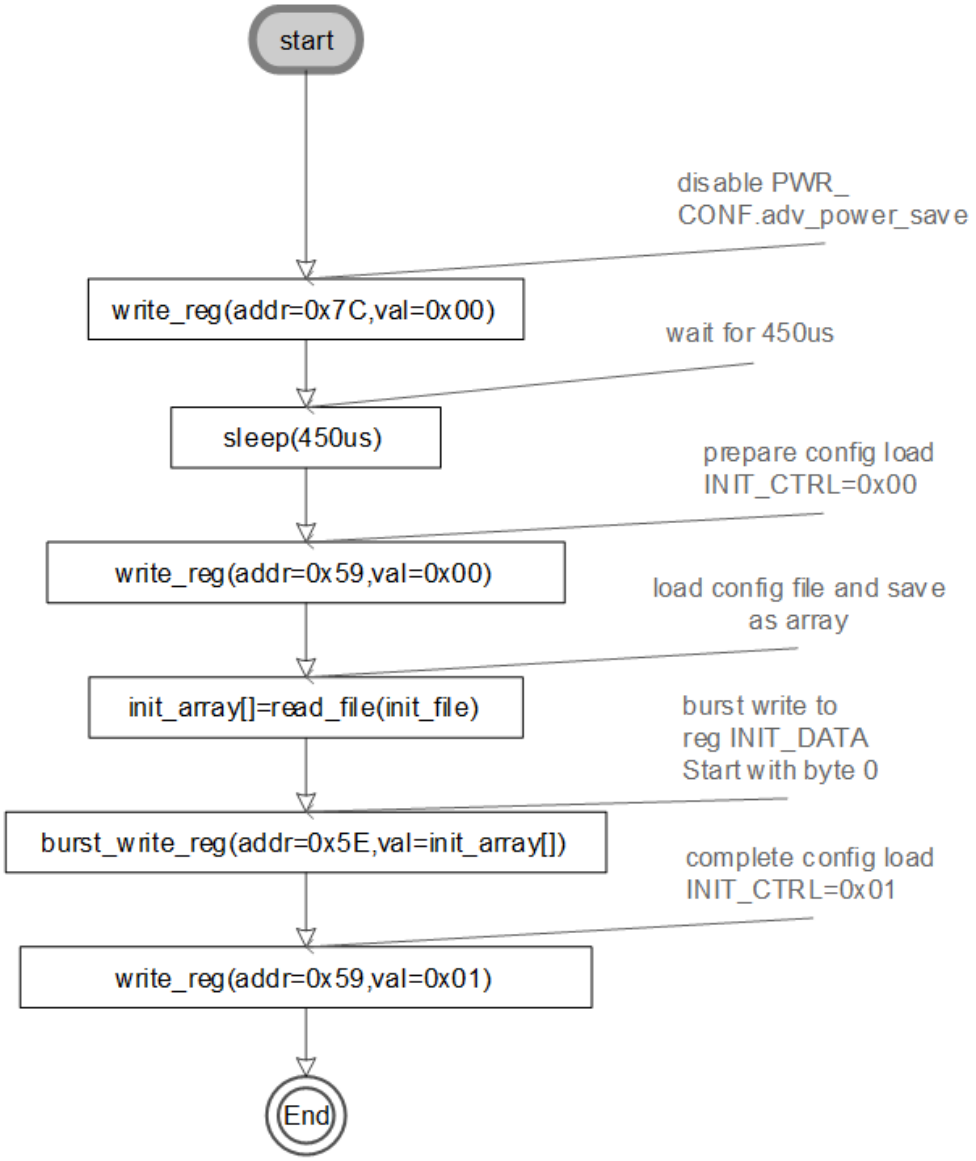
After correct power up by setting the correct voltage to the appropriate external pins, BMI270 enters automatically into the Power On Reset (POR) sequence. In order to properly use BMI270, certain steps from host processor front are needed. The most typical operations will be explained in the following application examples in form of flow diagrams.

1. *Testing communication and initializing BMI270*

a. Reading chip id CHIP_ID (0x24) (checking correct communication). The interface is coming up configured for I2C, the initial dummy read configures it to SPI.

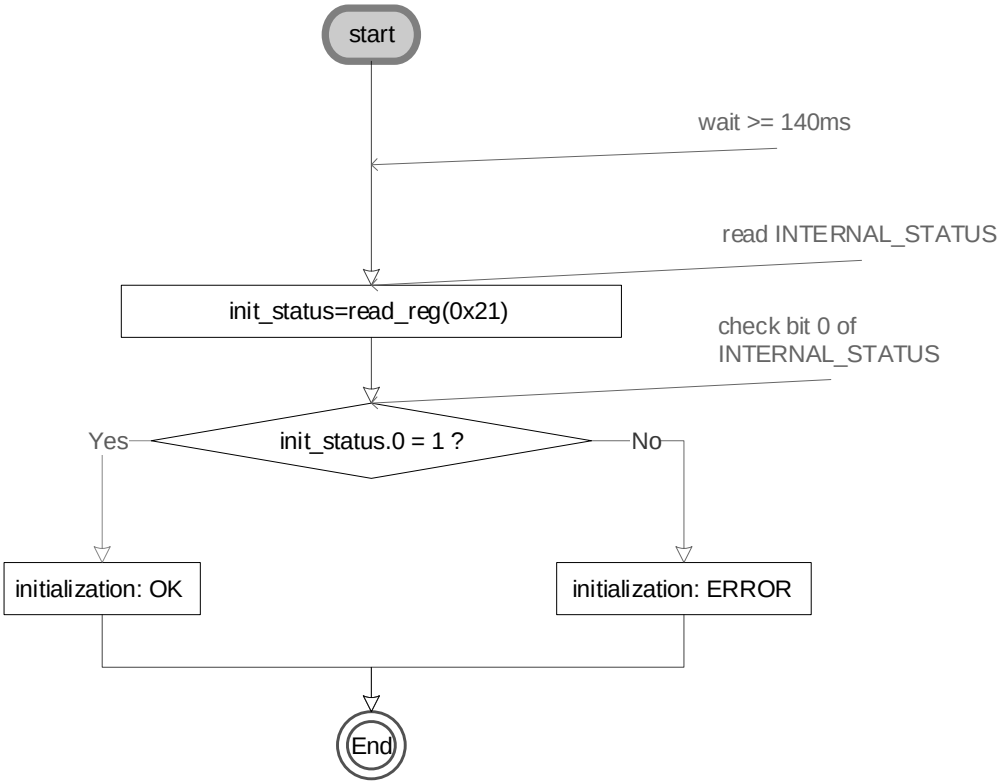


b. Performing initialization sequence[1]



[1] The bmi270_config_file in https://github.com/BoschSensortec/BMI270-Sensor-API/blob/master/bmi270_maximum_fifo.c

c. Checking the correct initialization status

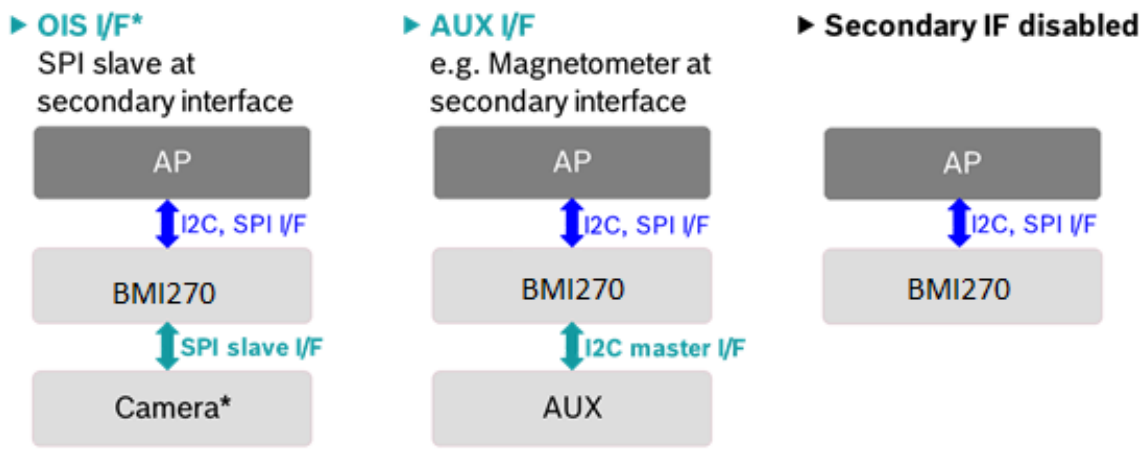


Note: To configure BMI270 in Low-power mode / Normal mode / Performance mode refer BMI270 data sheet

3. Functional Description

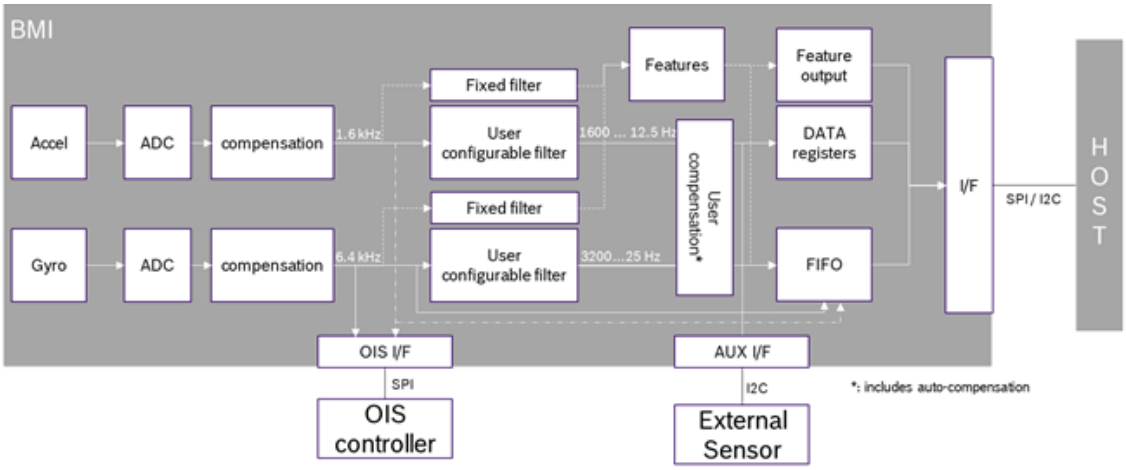
3.1. System Configurations

BMI270 has 14 external I/F pins and supports the SPI and I2C protocols on its primary interface to the host system. BMI270 supports on its secondary interface (I2C master) an auxiliary sensor configuration (e.g. a magnetometer) configuration. Both configurations work independent of the configuration (SPI/I2C) of the primary interface. If the secondary I/F is configured as AUX I/F, the sensor data of the IMU and the AUX sensor are synchronized.



3.2. Block Diagram

BMI270



For details regarding Supply Voltage, see BMI270 data sheet

3.3. **Power-On-Reset (POR) and Device Initialization**

During POR the voltages VDD/VDDIO are ramped to their respective target values. After reaching the target supply voltages, all registers are accessible after a delay of 450 µs.

After every POR or soft reset, the IMU remains in suspend mode. To get ready for operation the device must be initialized through the following procedure:

- Disable advanced power save mode: PWR_CONF.adv_power_save =0b0
- Wait for 450 µs (or 12 LSB of SENSORTIME_0)
- Write INIT_CTRL.init_ctrl = 0x00 – to prepare config load
- Upload configuration file
    - Burst write 328 Bytes of initialization data to Register INIT_DATA (start with byte 0 of initialization data)
    - The configuration file for Max FIFO is available on GitHub https://github.com/BoschSensortec/BMI270-Sensor-API/blob/master/bmi270_maximum_fifo.c
    - Optionally: Burst read configuration file from Register INIT_DATA and check correctness by comparing it to the data written to the register in the previous step.
- Write INIT_CTRL.init_ctrl = 0x01 – to complete config load.
  Note: This operation **must not** be performed more than once after POR or soft reset.
- Wait until Register INTERNAL_STATUS.message contains the value 0b0001. This will happen after at most 20 ms.

After the initialization sequence is completed, the power mode of the device is automatically set to “Configuration mode”. Now it is possible to switch to other power modes and the device is ready for operation as required and described in the following sections.

For details regarding switching to power modes, Sensor Data (Accel/Gyro and data processing in different modes) and possible filter settings, see BMI270 data sheet

3.4. **FIFO**

BMI270 supports the following FIFO operating modes:

- Streaming mode: overwrites oldest data on FIFO full condition
- FIFO mode: discards newest data on FIFO full condition

The FIFO size is 6 KB and supports the following interrupts:

- FIFO full interrupt
- FIFO watermark interrupt

FIFO is enabled for accelerometer data with FIFO_CONFIG_1.fifo_acc_en=0b1, for gyroscope data with FIFO_CONFIG_1.fifo_gyr_en=0b1, and auxiliary interface (e.g. magnetometer) data with FIFO_CONFIG_1.fifo_aux_en=0b1 (0b0=disabled).

The FIFO may be used in all power modes of BMI270. For further details on FIFO refer Chapter 4.7 of BMI270 data sheet

Bit	7	6	5	4	3	2	1	0
Content	fh_mode<1:0>		fh_parm<3:0>				reserved	

FIFO header contains information on fh_mode and fh_param as shown by bit-field definition.

3.5. General Interrupt Pin Configuration

Electrical Interrupt Pin Behavior

Both interrupt pins PIN1 and PIN2 can be configured to show the desired electrical behavior. Interrupt pins can be enabled in INT1_IO_CTRL.output_en and INT2_IO_CTRL.output_en. The characteristic of the output driver of the interrupt pins may be configured with bits INT1_IO_CTRL.od and INT2_IO_CTRL.od. By setting these bits to 0b1, the output driver shows open-drive characteristic, by setting the configuration bits to 0b0, the output driver shows push-pull characteristic.
The electrical behavior of the Interrupt pins, whenever an interrupt is triggered, can be configured as either “active-high” or “active-low” via INT1_IO_CTRL.lvl or INT2_IO_CTRL.lvl.

Both interrupt pins can be configured as input pins via INT1_IO_CTRL.input_en and INT2_IO_CTRL.input_en. This is necessary when FIFO tag feature is used (see Section FIFO synchronization with external interrupts” in BMI270 datasheet). If both are enabled, the input (e.g. marking FIFO) is driven by the interrupt output.

BMI270 supports edge and level triggered interrupt inputs, this can be configured through FIFO_CONFIG1.fifo_tag_int1_en and FIFO_CONFIG1.fifo_tag_int2_en.

BMI270 supports non-latched and latched interrupts modes for data ready, FIFO watermark, FIFO full, error, and the advanced feature interrupts. The mode is selected by INT_LATCH.int_latch. Non-latched interrupts are designed for systems using edge triggered interrupts, latched interrupts are designed for systems using level-triggered interrupts.

In latched mode an asserted interrupt status in INT_STATUS_0 (advanced feature interrupts) or INT_STATUS_1 (data ready, FIFO and error interrupts) and the selected pin are reset if the corresponding status register is read. If the interrupt activation condition still holds when the interrupt is reset, the interrupt status and pin are asserted again. If more than one interrupt pin is used in latched mode, all interrupts in INT_STATUS_0 should be mapped to one interrupt pin and all interrupts in INT_STATUS_1 should be mapped to the other interrupt pin. If just one interrupt pin is used all interrupts may be mapped to this interrupt pin.

In the non-latched mode the selected pin are reset as soon as the activation condition is not valid anymore. The interrupt status bits are active until read by the host.

Interrupt Pin Mapping

The data ready, FIFO watermark, FIFO full, error, and the advanced feature interrupts are mapped to the external INT1 or INT2 pins by setting the corresponding bits in the Registers INT_MAP_DATA, INT1_MAP_FEAT and INT2_MAP_FEAT. To unmap these interrupts, the corresponding bits must be reset.

Once an interrupt triggered the output pin, the host can derive the source of the interrupt of the corresponding status bit in the Register: INT_STATUS_0 and INT_STATUS_1.

4. Register Description

4.1. General Remarks

This section contains register definitions. REG[x]<y> denotes bit y in byte x in register REG. Val(Name) is the value contained in the register interpreted as non-negative binary number. When writing to reserved bits, '0' should be written if not stated different.

For most of the registers auto address increment applies for, with the exception of the registers below, which trap the address:

- FIFO_DATA
- INIT_DATA

Register read from a burst read must remain consistent. In order to ensure this, when a read starts in one register of a group, the registers in this group are shadowed:

- STATUS, DATA_x, SENSORTIME_x, TEMPERATURE_x, FIFO_LENGTH_x

The registers listed below are clear-on-read:

- ERR_REG
- STATUS.drdy_acc (cleared when DATA_9.acc_x_15_8 is read),
- STATUS.drdy_gyr (cleared when DATA_15.gyr_x_15_8 is read)
- STATUS.drdy_aux (cleared when DATA_1.aux_x_15_8 is read)
- EVENT
- INT_STATUS_0
- INT_STATUS_1

The register clearance happens, when bit 0 of the corresponding register is read.

4.2. **Register Map**

read/write	read only	write only	reserved

Corresponding to BMI270_maxfifo.tbin version 4.1, register map version 4.1

Register Address	Register Name	Default Value	7	6	5	4	3	2	1	0
0x7E	CMD	0x00	cmd							
0x7D	PWR_CTRL	0x00	reserved				temp_en	acc_en	gyr_en	aux_en
0x7C	PWR_CONF	0x03	reserved					fup_en	fifo_self_wake_up	adv_power_save
0x7B	-	-	reserved							
...	-	-	reserved							
0x78	-	-	reserved							
0x77	OFFSET_6	0x00	gyr_gain_en	gyr_off_en	gyr_usr_off_z_9_8		gyr_usr_off_y_9_8		gyr_usr_off_x_9_8	
0x76	OFFSET_5	0x00	gyr_usr_off_z_7_0							
0x75	OFFSET_4	0x00	gyr_usr_off_y_7_0							
0x74	OFFSET_3	0x00	gyr_usr_off_x_7_0							
0x73	OFFSET_2	0x00	off_acc_z							
0x72	OFFSET_1	0x00	off_acc_y							
0x71	OFFSET_0	0x00	off_acc_x							
0x70	NV_CONF	0x00	reserved				acc_off_en	i2c_wdt_en	i2c_wdt_sel	spi_en
0x6F	-	-	reserved							
0x6E	GYR_SELF_TEST_AXES	0x00	reserved				gyr_axis_z_ok	gyr_axis_y_ok	gyr_axis_x_ok	gyr_st_axes_done
0x6D	ACC_SELF_TEST	0x00	reserved				acc_self_test_amp	acc_self_test_sign	reserved	acc_self_test_en
0x6C	DRV	0xFF	io_pad_i2c_b2	io_pad_drv2			io_pad_i2c_b1	io_pad_drv1		
0x6B	IF_CONF	0x00	reserved		aux_en	ois_en	reserved		spi3_ois	spi3
0x6A	NVM_CONF	0x00	reserved						nvm_prog_en	reserved
0x69	-	0x00	reserved							
0x68	AUX_IF_TRIM	0x01	reserved						asda_pupsel	
0x67	-	-	reserved							
...	-	-	reserved							
0x60	-	-	reserved							

0x5F	INTERNAL_ERROR	0x00	reserved			feat_eng_disabled	reserved	int_err_2	int_err_1	reserved
0x5E	INIT_DATA	0x00	data							
0x5D	-	-	reserved							
0x5C	INIT_ADDR_1	0x00	base_11_4							
0x5B	INIT_ADDR_0	0x00	reserved				base_0_3			
0x5A	-	-	reserved							
0x59	INIT_CTRL	0x00	init_ctrl							
0x58	INT_MAP_DATA	0x00	err_int2	drdy_int2	fwm_int2	ffull_int2	err_int1	drdy_int1	fwm_int1	ffull_int1
0x57	INT2_MAP_FEAT	0x00	reserved							
0x56	INT1_MAP_FEAT	0x00	reserved							
0x55	INT_LATCH	0x00	reserved							int_latch
0x54	INT2_IO_CTRL	0x00	reserved			input_en	output_en	od	lvl	reserved
0x53	INT1_IO_CTRL	0x00	reserved			input_en	output_en	od	lvl	reserved
0x52	ERR_REG_MSK	0x00	aux_err	fifo_err	reserved	internal_err				fatal_err
0x51	-	-	reserved							
0x50	-	-	reserved							
0x4F	AUX_WR_DATA	0x02	write_data							
0x4E	AUX_WR_ADDR	0x4C	write_addr							
0x4D	AUX_RD_ADDR	0x42	read_addr							
0x4C	AUX_IF_CONF	0x83	aux_manual_en	aux_fcu_write_en	reserved		man_rd_burst		aux_rd_burst	
0x4B	AUX_DEV_ID	0x20	i2c_device_addr							reserved
0x4A	SATURATION	0x00	reserved			gyr_z	gyr_y	gyr_x	acc_z	acc_y	acc_x
0x49	FIFO_CONFIG_1	0x10	fifo_gyr_en	fifo_acc_en	fifo_aux_en	fifo_header_en	fifo_tag_int2_en		fifo_tag_int1_en	
0x48	FIFO_CONFIG_0	0x02	reserved						fifo_time_en	fifo_stop_on_full
0x47	FIFO_WTM_1	0x02	reserved			fifo_water_mark_12_8				
0x46	FIFO_WTM_0	0x00	fifo_water_mark_7_0							
0x45	FIFO_DOWNS	0x88	acc_fifo_filt_data	acc_fifo_downs			gyr_fifo_filt_data	gyr_fifo_downs		
0x44	AUX_CONF	0x46	aux_offset				aux_odr			

0x43	GYR_RANGE	0x00	reserved				ois_range	gyr_range
0x42	GYR_CONF	0xA9	gyr_filter_perf	gyr_noise_perf	gyr_bwp		gyr_odr	
0x41	ACC_RANGE	0x02	reserved					acc_range
0x40	ACC_CONF	0xA8	acc_filter_perf	acc_bwp			acc_odr	
0x3F	-	-	reserved					
...	-	-	reserved					
0x27	-	-	reserved					
0x26	FIFO_DATA	0x00	fifo_data					
0x25	FIFO_LENGTH_1	0x00	reserved	fifo_byte_counter_13_8				
0x24	FIFO_LENGTH_0	0x00	fifo_byte_counter_7_0					
0x23	TEMPERATURE_1	0x80	tmp_data_15_8					
0x22	TEMPERATURE_0	0x00	tmp_data_7_0					
0x21	INTERNAL_STATUS	0x00	Reserved				message	
0x20	Reserved	0x00	Reserved					
0x1F	Reserved	0x00	Reserved					
0x1E	GYR_CAS	0x00	reserved	factor_zx				
0x1D	INT_STATUS_1	0x00	acc_drdy_int	gyr_drdy_int	aux_drdy_int	reserved	err_int	fwm_int	ffull_int
0x1C	INT_STATUS_0	0x00	reserved					
0x1B	EVENT	0x01	reserved			error_code	reserved	por_detected
0x1A	SENSORTIME_2	0x00	sensor_time_23_16					
0x19	SENSORTIME_1	0x00	sensor_time_15_8					
0x18	SENSORTIME_0	0x00	sensor_time_7_0					
0x17	DATA_19	0x00	gyr_z_15_8					
0x16	DATA_18	0x00	gyr_z_7_0					
0x15	DATA_17	0x00	gyr_y_15_8					
0x14	DATA_16	0x00	gyr_y_7_0					
0x13	DATA_15	0x00	gyr_x_15_8					
0x12	DATA_14	0x00	gyr_x_7_0					
0x11	DATA_13	0x00	acc_z_15_8					
0x10	DATA_12	0x00	acc_z_7_0					
0x0F	DATA_11	0x00	acc_y_15_8					
0x0E	DATA_10	0x00	acc_y_7_0					
0x0D	DATA_9	0x00	acc_x_15_8					
0x0C	DATA_8	0x00	acc_x_7_0					
0x0B	DATA_7	0x00	aux_r_15_8					

0x0A	DATA_6	0x00	aux_r_7_0						
0x09	DATA_5	0x00	aux_z_15_8						
0x08	DATA_4	0x00	aux_z_7_0						
0x07	DATA_3	0x00	aux_y_15_8						
0x06	DATA_2	0x00	aux_y_7_0						
0x05	DATA_1	0x00	aux_x_15_8						
0x04	DATA_0	0x00	aux_x_7_0						
0x03	STATUS	0x10	drdy_acc	drdy_gyr	drdy_aux	cmd_rdy	reserved	aux_busy	reserved
0x02	ERR_REG	0x00	aux_err	fifo_err	reserved	internal_err			fatal_err
0x01	-	-	reserved						
0x00	CHIP_ID	0x24	chip_id						

Register (0x00) CHIP_ID

DESCRIPTION: Chip identification code
RESET: 0x24
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x00		CHIP_ID		0x24	
	7...0	chip_id	Chip identification code	0x24	R

Register (0x02) ERR_REG

DESCRIPTION: Reports sensor error conditions
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x02		ERR_REG		0x00	
	0	fatal_err	Fatal Error, chip is not in operational state (Boot-, power-system). This flag will be reset only by power-on-reset or softreset.	0x0	R
	4...1	internal_err	Internal error, please contact your Bosch Sensortec regional support team.	0x0	R
	6	fifo_err	Error when a frame is read in streaming mode (so skipping is not possible) and fifo is overfilled (with virtual and/or regular frames). This flag will be reset when read.	0x0	R
	7	aux_err	Error in I2C-Master detected. This flag will be reset when read.	0x0	R

Register (0x03) STATUS

DESCRIPTION: Sensor status flags
RESET: 0x10
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x03		STATUS		0x10	
	2	aux_busy	'1'('0') indicate a (no) Auxiliary sensor interface operation is ongoing triggered via AUX_RD_ADDR, AUX_WR_ADDR or from FCU.	0x0	R
	4	cmd_rdy	CMD decoder status. `0´ -> Command in progress `1´ -> Command decoder is ready to accept a new command	0x1	R
	5	drdy_aux	Data ready for Auxiliary sensor. It gets reset, when one Auxiliary sensor DATA register is read out	0x0	R
	6	drdy_gyr	Data ready for Gyroscope. It gets reset, when one Gyroscope DATA register is read out	0x0	R
	7	drdy_acc	Data ready for Accelerometer. It gets reset, when one Accelerometer DATA register is read out	0x0	R

Register (0x04) DATA_0

DESCRIPTION: AUX_X(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x04		DATA_0		0x00	
	7...0	aux_x_7_0	copy of register Val(AUX_IF[1]) in Auxiliary sensor register map.	0x0	R

Register (0x05) DATA_1

DESCRIPTION: AUX_X(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x05		DATA_1		0x00	
	7...0	aux_x_15_8	copy of register Val(AUX_IF[1])+1 in Auxiliary sensor register map	0x0	R

Register (0x06) DATA_2

DESCRIPTION: AUX_Y(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x06		DATA_2		0x00	
	7...0	aux_y_7_0	copy of register Val(AUX_IF[1])+2 in Auxiliary sensor register map	0x0	R

Register (0x07) DATA_3

DESCRIPTION: AUX_Y(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x07		DATA_3		0x00	
	7...0	aux_y_15_8	copy of register Val(AUX_IF[1])+3 in Auxiliary sensor register map	0x0	R

Register (0x08) DATA_4

DESCRIPTION: AUX_Z(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x08		DATA_4		0x00	
	7...0	aux_z_7_0	copy of register Val(AUX_IF[1])+4 in Auxiliary sensor register map	0x0	R

Register (0x09) DATA_5

DESCRIPTION: AUX_Z(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x09		DATA_5		0x00	
	7...0	aux_z_15_8	copy of register Val(AUX_IF[1])+5 in Auxiliary sensor register map	0x0	R

Register (0x0A) DATA_6

DESCRIPTION: AUX_R(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x0A		DATA_6		0x00	
	7...0	aux_r_7_0	copy of register Val(AUX_IF[1])+6 in Auxiliary sensor register map	0x0	R

Register (0x0B) DATA_7

DESCRIPTION: AUX_R(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x0B		DATA_7		0x00	
	7...0	aux_r_15_8	copy of register Val(AUX_IF[1])+7 in Auxiliary sensor register map	0x0	R

Register (0x0C) DATA_8

DESCRIPTION: ACC_X(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x0C		DATA_8		0x00	
	7...0	acc_x_7_0		0x0	R

Register (0x0D) DATA_9

DESCRIPTION: ACC_X(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x0D		DATA_9		0x00	
	7...0	acc_x_15_8		0x0	R

Register (0x0E) DATA_10

DESCRIPTION: ACC_Y(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x0E		DATA_10		0x00	
	7...0	acc_y_7_0		0x0	R

Register (0x0F) DATA_11

DESCRIPTION: ACC_Y(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x0F		DATA_11		0x00	
	7...0	acc_y_15_8		0x0	R

Register (0x10) DATA_12

DESCRIPTION: ACC_Z(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x10		DATA_12		0x00	
	7...0	acc_z_7_0		0x0	R

Register (0x11) DATA_13

DESCRIPTION: ACC_Z(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x11		DATA_13		0x00	
	7...0	acc_z_15_8		0x0	R

Register (0x12) DATA_14

DESCRIPTION: GYR_X(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x12		DATA_14		0x00	
	7...0	gyr_x_7_0		0x0	R

Register (0x13) DATA_15

DESCRIPTION: GYR_X(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x13		DATA_15		0x00	
	7...0	gyr_x_15_8		0x0	R

Register (0x14) DATA_16

DESCRIPTION: GYR_Y(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x14		DATA_16		0x00	
	7...0	gyr_y_7_0		0x0	R

Register (0x15) DATA_17

DESCRIPTION: GYR_Y(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x15		DATA_17		0x00	
	7...0	gyr_y_15_8		0x0	R

Register (0x16) DATA_18

DESCRIPTION: GYR_Z(LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x16		DATA_18		0x00	
	7...0	gyr_z_7_0		0x0	R

Register (0x17) DATA_19

DESCRIPTION: GYR_Z(MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x17		DATA_19		0x00	
	7...0	gyr_z_15_8		0x0	R

Register (0x18) SENSORTIME_0

DESCRIPTION: Sensor time <7:0>
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x18		SENSORTIME_0		0x00	
	7...0	sensor_time_7_0	Sensor time <7:0>	0x0	R

Register (0x19) SENSORTIME_1

DESCRIPTION: Sensor time <15:8>
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x19		SENSORTIME_1		0x00	
	7...0	sensor_time_15_8	Sensor time <15:8>.	0x0	R

Register (0x1A) SENSORTIME_2

DESCRIPTION: Sensor time <23:16>
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x1A		SENSORTIME_2		0x00	
	7...0	sensor_time_23_16	Sensor time <23:16> The sensor time is a 24 bit counter available in suspend, low power, and normal mode. The value of the SENSORTIME register is shadowed, when it is read in a burst read with the data register at the beginning of the operation and the shadowed value is returned. When the fifo is read the register is shadowed, whenever a new frame is read. The resolution of the sensor_time is 39.0625 us, and it is synchrounous to ODR. The register wraps if it reaches 0xFFFFFF.	0x0	R

Register (0x1B) EVENT

DESCRIPTION: Sensor event flags. Will be cleared on read when bit 0 is sent out over the bus.
RESET: 0x01
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x1B		EVENT		0x01	
	0	por_detected	'1' after device power up or softreset, '0' after status read.	0x1	R
	4...2	error_code	Error codes for persistent errors **Value** **Name** **Description** 0x00 no_error no error is reported 0x01 acc_err error in Register ACC_CONF 0x02 gyr_err error in Register GYR_CONF 0x03 acc_and_gyr_err error in Registers ACC_GYR & GYR_CONF	0x0	R

Register (0x1C) INT_STATUS_0

DESCRIPTION: Reserved
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x1C		INT_STATUS_0		0x00	
	7...0	reserved	Reserved	0x0	R

Register (0x1D) INT_STATUS_1

DESCRIPTION: Interrupt Status 1. Will be cleared on read when bit 0 is sent out over the bus.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x1D		INT_STATUS_1		0x00	
	0	ffull_int	FIFO Full Interrupt	0x0	R
	1	fwm_int	FIFO Watermark Interrupt	0x0	R
	2	err_int	ERROR Interrupt	0x0	R
	5	aux_drdy_int	Auxiliary Data Ready Interrupt	0x0	R
	6	gyr_drdy_int	Gyroscope Data Ready Interrupt	0x0	R
	7	acc_drdy_int	Accelerometer Data Ready Interrupt	0x0	R

Register (0x1E) GYR_CAS

DESCRIPTION: Register for gyroscope data post processing
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x1E		GYR_CAS		0x00	
	6...0	factor_zx	Factor to further optimize the gyroscope performance	0x0	R

Register (0x1F) Reserved

DESCRIPTION: Reserved
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x1F		Reserved		0x00	
	7...0	Reserved	Reserved	0x0	R

Register (0x20) Reserved

DESCRIPTION: Reserved
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x20		Reserved		0x00	
	7...0	Reserved	Reserved	0x0	R

Register (0x21) INTERNAL_STATUS

DESCRIPTION: Error bits and message indicating internal status
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x21		INTERNAL_STATUS		0x00	
	3...0	message	Internal Status Message **Value** / **Name** / **Description** 0x00 / not_init / ASIC is not initialized 0x01 / init_ok / ASIC initialized 0x02 / init_err / Initialization error 0x03 / drv_err / Invalid driver 0x04 / sns_stop / Sensor stopped 0x05 / nvm_error / Internal error while accessing NVM 0x06 / start_up_error / Internal error while accessing NVM and Initialization error 0x07 / compat_error / Compatibility error	0x0	R
	7...4	Reserved	Reserved	0x0	R

Register (0x22) TEMPERATURE_0

DESCRIPTION: Temperature LSB; The temperature is disabled when all sensors are in suspend. The output word of the 16-bit temperature sensor is valid if the Gyroscope is in normal mode, i.e. gyr_pmu_status=1. The resolution is 1/2^9 K/LSB. The absolute accuracy of the temperature is in the order of:

0x7FFF -> 87-1/2^9 °C
0x0000 -> 23°C
0x8001 -> -41+1/2^9 °C
0x8000 -> invalid

If the Gyroscope is in normal mode (see register PMU_STATUS), the temperature is updated every 10 ms (+-12%), if the gyroscope is in standby mode or fast-power up mode, the temperature is updated ever 1.28 s aligned with bit 15 of the register SENSORTIME.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x22		TEMPERATURE_0		0x00	
	7...0	tmp_data_7_0	Temperature value.	0x0	R

Register (0x23) TEMPERATURE_1

DESCRIPTION: Contains the MSBs of temperature sensor value
RESET: 0x80
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x23		TEMPERATURE_1		0x80	
	7...0	tmp_data_15_8	Temperature LSBs.	0x80	R

Register (0x24) FIFO_LENGTH_0

DESCRIPTION: FIFO byte count register (LSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x24		FIFO_LENGTH_0		0x00	
	7...0	fifo_byte_counter_7_0	Current fill level of FIFO buffer This includes the skip frame for a full fifo. An empty FIFO corresponds to 0x000. The byte counter may be reset by reading out all frames from the FIFO buffer or when the FIFO is reset through the register CMD. The byte counter is updated each time a complete frame was read or written.	0x0	R

Register (0x25) FIFO_LENGTH_1

DESCRIPTION: FIFO byte count register (MSB)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x25		FIFO_LENGTH_1		0x00	
	5...0	fifo_byte_counter_13_8	FIFO byte counter bits 13..8	0x0	R

Register (0x26) FIFO_DATA

DESCRIPTION: FIFO data output register
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x26		FIFO_DATA		0x00	
	7...0	fifo_data	FIFO read data (8 bits) Data format depends on the setting of register FIFO_CONFIG. The FIFO data are organized in frames. The new data flag is preserved. Read burst access must be used, the address will not increment when the read burst reads at the address of FIFO_DATA. When a frame is only partially read out it is retransmitted including the header at the next readout.	0x0	R

Register (0x40) ACC_CONF

DESCRIPTION: Sets the output data rate, the bandwidth, and the performance mode of the acceleration sensor
RESET: 0xA8
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x40		ACC_CONF		0xA8	
	3...0	acc_odr	ODR in Hz. The output data rate is independent of the power mode setting for the sensor **Value** **Name** **Description** 0x00 reserved Reserved 0x01 odr_0p78 25/32 0x02 odr_1p5 25/16 0x03 odr_3p1 25/8 0x04 odr_6p25 25/4 0x05 odr_12p5 25/2 0x06 odr_25 25 0x07 odr_50 50 0x08 odr_100 100 0x09 odr_200 200 0x0a odr_400 400 0x0b odr_800 800 0x0c odr_1k6 1600 0x0d odr_3k2 Reserved 0x0e odr_6k4 Reserved 0x0f odr_12k8 Reserved	0x8	RW
	6...4	acc_bwp	Bandwidth parameter determines filter configuration (acc_filt_perf=1) and averaging for undersampling mode (acc_filt_perf=0) **Value** **Name** **Description** 0x00 osr4_avg1 acc_filt_perf = 1 -> OSR4 mode; acc_filt_perf = 0 -> no averaging 0x01 osr2_avg2 acc_filt_perf = 1 -> OSR2 mode; acc_filt_perf = 0 -> average 2 samples 0x02 norm_avg4 acc_filt_perf = 1 -> normal mode; acc_filt_perf = 0 -> average 4 samples 0x03 cic_avg8 acc_filt_perf = 1 -> CIC mode; acc_filt_perf = 0 -> average 8 samples	0x2	RW

			0x04	res_avg16	acc_filt_perf = 1 -> Reserved; acc_filt_perf = 0 -> average 16 samples		
			0x05	res_avg32	acc_filt_perf = 1 -> Reserved; acc_filt_perf = 0 -> average 32 samples		
			0x06	res_avg64	acc_filt_perf = 1 -> Reserved; acc_filt_perf = 0 -> average 64 samples		
			0x07	res_avg128	acc_filt_perf = 1 -> Reserved; acc_filt_perf = 0 -> average 128 samples		
	7	acc_filter_perf	Select accelerometer filter performance mode: **Value** **Name** **Description** 0x00 ulp power optimized 0x01 hp performance opt.			0x1	RW

Register (0x41) ACC_RANGE

DESCRIPTION: Selection of the Accelerometer g-range
RESET: 0x02
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x41		ACC_RANGE		0x02	
	1...0	acc_range	Accelerometer g-range **Value** **Name** **Description** 0x00 range_2g +/-2g 0x01 range_4g +/-4g 0x02 range_8g +/-8g 0x03 range_16g +/-16g	0x2	RW

Register (0x42) GYR_CONF

DESCRIPTION: Sets the output data rate and the bandwidth of the Gyroscope in the sensor
RESET: 0xA9
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x42		GYR_CONF		0xA9	
	3...0	gyr_odr	ODR in Hz **Value Name Description** 0x00 reserved Reserved 0x01 odr_0p78 Reserved 0x02 odr_1p5 Reserved 0x03 odr_3p1 Reserved 0x04 odr_6p25 Reserved 0x05 odr_12p5 Reserved 0x06 odr_25 25 0x07 odr_50 50 0x08 odr_100 100 0x09 odr_200 200 0x0a odr_400 400 0x0b odr_800 800 0x0c odr_1k6 1600 0x0d odr_3k2 3200 0x0e odr_6k4 Reserved 0x0f odr_12k8 Reserved	0x9	RW
	5...4	gyr_bwp	The Gyroscope bandwidth coefficient defines the 3 dB cutoff frequency of the low pass filter for the sensor data **Value Name Description** 0x00 osr4 OSR4 mode 0x01 osr2 OSR2 mode 0x02 norm normal mode 0x03 res reserved	0x2	RW
	6	gyr_noise_perf	Select noise performance: **Value Name Description** 0x00 ulp power optimized 0x01 hp performance opt.	0x0	RW
	7	gyr_filter_perf	Select gyroscope filter performance mode: **Value Name Description** 0x00 ulp power optimized 0x01 hp performance opt.	0x1	RW

Register (0x43) GYR_RANGE

DESCRIPTION: Defines the Gyroscope angular rate measurement range
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x43		GYR_RANGE		0x00	
	2...0	gyr_range	Full scale, Resolution: applies to filtered FIFO data and DATA registers. **Value** **Name** **Description** 0x00 range_2000 +/-2000dps, 16.4 LSB/dps 0x01 range_1000 +/-1000dps, 32.8 LSB/dps 0x02 range_500 +/-500dps, 65.6 LSB/dps 0x03 range_250 +/-250dps, 131.2 LSB/dps 0x04 range_125 +/-125dps, 262.4 LSB/dps	0x0	RW
	3	ois_range	Full scale, Resolution: applies to pre-filtered FIFO data and OIS data. **Value** **Name** **Description** 0x00 range_250 +/-250dps, 131.2 LSB/dps 0x01 range_2000 +/-2000dps, 16.4 LSB/dps	0x0	RW

Register (0x44) AUX_CONF

DESCRIPTION: Sets the output data rate of the Auxiliary sensor interface
RESET: 0x46
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x44		AUX_CONF		0x46	
	3...0	aux_odr	define the poll rate for the magnetometer attached to the Auxiliary sensor interface. This is independent of the power mode setting for the sensor. The output data rate in Hz. In addition to setting the poll rate, it is required to configure the Auxiliary sensor properly using the AUX_IF_CONF register. **Value Name Description** 0x00 reserved Reserved 0x01 odr_0p78 25/32 0x02 odr_1p5 25/16 0x03 odr_3p1 25/8 0x04 odr_6p25 25/4 0x05 odr_12p5 25/2 0x06 odr_25 25 0x07 odr_50 50 0x08 odr_100 100 0x09 odr_200 200 0x0a odr_400 400 0x0b odr_800 800 0x0c odr_1k6 Reserved 0x0d odr_3k2 Reserved 0x0e odr_6k4 Reserved 0x0f odr_12k8 Reserved	0x6	RW
	7...4	aux_offset	trigger-readout offset in units of 2.5 ms. If set to zero, the offset is maximum, i.e. after readout a trigger is issued immediately.	0x4	RW

Register (0x45) FIFO_DOWNS

DESCRIPTION: Configure Gyroscope and Accelerometer downsampling rates for FIFO
RESET: 0x88
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x45		FIFO_DOWNS		0x88	
	2...0	gyr_fifo_downs	Downsampling for Gyroscope (2**downs_gyro)	0x0	RW
	3	gyr_fifo_filt_data	selects filtered or unfiltered Gyroscope data for fifo **Value Name Description** 0x00 unfiltered Unfiltered data 0x01 filtered Filtered data	0x1	RW
	6...4	acc_fifo_downs	Downsampling for Accelerometer (2**downs_accel)	0x0	RW
	7	acc_fifo_filt_data	selects filtered or unfiltered Accelerometer data for fifo **Value Name Description** 0x00 unfiltered Unfiltered data 0x01 filtered Filtered data	0x1	RW

Register (0x46) FIFO_WTM_0

DESCRIPTION: FIFO Watermark level LSB
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x46		FIFO_WTM_0		0x00	
	7...0	fifo_water_mark_7_0	Trigger an interrupt when FIFO contains fifo_water_mark_7_0+fifo_water_mark_12_8*256 bytes	0x0	RW

Register (0x47) FIFO_WTM_1

DESCRIPTION: FIFO Watermark level MSB and frame content configuration
RESET: 0x02
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x47		FIFO_WTM_1		0x02	
	4...0	fifo_water_mark_12_8	Trigger an interrupt when FIFO contains fifo_water_mark_7_0+fifo_water_mark_12_8*256 bytes	0x2	RW

Register (0x48) FIFO_CONFIG_0

DESCRIPTION: FIFO frame content configuration
RESET: 0x02
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x48		FIFO_CONFIG_0		0x02	
	0	fifo_stop_on_full	Stop writing samples into FIFO when FIFO is full. **Value** **Name** **Description** 0x00 disable do not stop writing to FIFO when full 0x01 enable Stop writing into FIFO when full.	0x0	RW
	1	fifo_time_en	Return sensortime frame after the last valid data frame. **Value** **Name** **Description** 0x00 disable do not return sensortime frame 0x01 enable return sensortime frame	0x1	RW

Register (0x49) FIFO_CONFIG_1

DESCRIPTION: FIFO frame content configuration
RESET: 0x10
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x49		FIFO_CONFIG_1		0x10	
	1...0	fifo_tag_int1_en	FIFO interrupt 1 tag enable **Value** **Name** **Description** 0x00 int_edge enable tag on rising edge of int pin 0x01 int_level enable tag on level value of int pin 0x02 acc_sat enable tag on saturation of accelerometer data 0x03 gyr_sat enable tag on saturation of gyroscope data	0x0	RW
	3...2	fifo_tag_int2_en	FIFO interrupt 2 tag enable **Value** **Name** **Description** 0x00 int_edge enable tag on rising edge of int pin 0x01 int_level enable tag on level value of int pin 0x02 acc_sat enable tag on saturation of accelerometer data 0x03 gyr_sat enable tag on saturation of gyroscope data	0x0	RW
	4	fifo_header_en	FIFO frame header enable **Value** **Name** **Description** 0x00 disable no header is stored (output data rate of all enabled sensors need to be identical) 0x01 enable header is stored	0x1	RW
	5	fifo_aux_en	Store Auxiliary sensor data in FIFO (all 3 axes) **Value** **Name** **Description** 0x00 disable no Auxiliary sensor data is stored 0x01 enable Auxiliary sensor data is stored	0x0	RW

	6	fifo_acc_en	Store Accelerometer data in FIFO (all 3 axes) **Value** **Name** **Description** 0x00 disable no Accelerometer data is stored 0x01 enable Accelerometer data is stored	0x0	RW
	7	fifo_gyr_en	Store Gyroscope data in FIFO (all 3 axes) **Value** **Name** **Description** 0x00 disable no Gyroscope data is stored 0x01 enable Gyroscope data is stored	0x0	RW

Register (0x4A) SATURATION

DESCRIPTION: Contains the information if one of the raw data samples used to generate current filtered data sample has been saturated (reached 0x8001 or 0x7FFF). The register is updated synchronous to the corresponding data registers in DATA_0..19.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x4A		SATURATION		0x00	
	0	acc_x	ACC X-axis raw data saturation flag.	0x0	R
	1	acc_y	ACC Y-axis raw data saturation flag.	0x0	R
	2	acc_z	ACC Z-axis raw data saturation flag.	0x0	R
	3	gyr_x	GYR X-axis raw data saturation flag.	0x0	R
	4	gyr_y	GYR Y-axis raw data saturation flag.	0x0	R
	5	gyr_z	GYR Z-axis raw data saturation flag.	0x0	R

Register (0x4B) AUX_DEV_ID

DESCRIPTION: Auxiliary interface device_id
RESET: 0x20
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x4B		AUX_DEV_ID		0x20	
	7...1	i2c_device_addr	I2C device address of Auxiliary sensor	0x10	RW

Register (0x4C) AUX_IF_CONF

DESCRIPTION: Auxiliary interface configuration register
RESET: 0x83
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x4C		AUX_IF_CONF		0x83	
	1...0	aux_rd_burst	Burst data length (1,2,6,8 byte) **Value Name Description** 0x00 BL1 Burst length 1 0x01 BL2 Burst length 2 0x02 BL6 Burst length 6 0x03 BL8 Burst length 8	0x3	RW
	3...2	man_rd_burst	Manual burst data length (1,2,6,8 byte) **Value Name Description** 0x00 BL1 Burst length 1 0x01 BL2 Burst length 2 0x02 BL6 Burst length 6 0x03 BL8 Burst length 8	0x0	RW
	6	aux_fcu_write_en	enables FCU write command on AUX IF for auxiliary sensors that need a trigger.	0x0	RW
	7	aux_manual_en	switches auxiliary interface between automatic and manual mode. In manual mode all read and write operations on auxiliary interface must be triggered manually; in automatic mode (aux_manual_en = “0”) FCU triggers read and write operations periodically (as programmed by user).	0x1	RW

Register (0x4D) AUX_RD_ADDR

DESCRIPTION: Auxiliary interface read address
RESET: 0x42
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x4D		AUX_RD_ADDR		0x42	
	7...0	read_addr	Address to read. In manual mode it triggers the read operation.	0x42	RW

Register (0x4E) AUX_WR_ADDR

DESCRIPTION: Auxiliary interface write address
RESET: 0x4C
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x4E		AUX_WR_ADDR		0x4C	
	7...0	write_addr	Address to write. In manual mode it triggers the write operation.	0x4C	RW

Register (0x4F) AUX_WR_DATA

DESCRIPTION: Auxiliary interface write data
RESET: 0x02
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x4F		AUX_WR_DATA		0x02	
	7...0	write_data	Data to write	0x2	RW

Register (0x52) ERR_REG_MSK

DESCRIPTION: Defines which error flag will trigger the error interrupt once enabled
'1' - use to generate the error interrupt
'0' - do not use to generate error interrupt
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x52		ERR_REG_MSK		0x00	
	0	fatal_err	Use fatal error to generate the error interrupt.	0x0	RW
	4...1	internal_err	Use internal error to generate the error interrupt	0x0	RW
	6	fifo_err	Use fifo error to generate the error interrupt.	0x0	RW
	7	aux_err	Use aux interface error to generate the error interrupt.	0x0	RW

Register (0x53) INT1_IO_CTRL

DESCRIPTION: Configure the electrical behavior of the interrupt pin INT1
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x53		INT1_IO_CTRL		0x00	
	1	lvl	Configure level of INT1 pin **Value Name Description** 0x00 active_low active low 0x01 active_high active high	0x0	RW
	2	od	Configure behaviour of INT1 pin **Value Name Description** 0x00 push_pull push-pull 0x01 open_drain open drain	0x0	RW
	3	output_en	Output enable for INT1 pin **Value Name Description** 0x00 off Output disabled 0x01 on Output enabled	0x0	RW
	4	input_en	Input enable for INT1 pin **Value Name Description** 0x00 off Input disabled 0x01 on Input enabled	0x0	RW

Register (0x54) INT2_IO_CTRL

DESCRIPTION: Configure the electrical behavior of the interrupt pin INT2
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x54		INT2_IO_CTRL		0x00	
	1	lvl	Configure level of INT2 pin **Value Name Description** 0x00 active_low active low 0x01 active_high active high	0x0	RW
	2	od	Configure behaviour of INT2 pin **Value Name Description** 0x00 push_pull push-pull 0x01 open_drain open drain	0x0	RW
	3	output_en	Output enable for INT2 pin **Value Name Description** 0x00 off Output disabled 0x01 on Output enabled	0x0	RW
	4	input_en	Input enable for INT2 pin **Value Name Description** 0x00 off Input disabled 0x01 on Input enabled	0x0	RW

Register (0x55) INT_LATCH

DESCRIPTION: Configure interrupt modes
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x55		INT_LATCH		0x00	
	0	int_latch	Latched/non-latched interrupt modes **Value Name Description** 0x00 none non latched 0x01 permanent permanent latched	0x0	RW

Register (0x56) INT1_MAP_FEAT

DESCRIPTION: Reserved
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x56		INT1_MAP_FEAT		0x00	
	7...0	reserved	Reserved	0x0	RW

Register (0x57) INT2_MAP_FEAT

DESCRIPTION: Reserved
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x57		INT2_MAP_FEAT		0x00	
	7...0	reserved	Reserved	0x0	RW

Register (0x58) INT_MAP_DATA

DESCRIPTION: Data Interrupt mapping for both INT pins
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x58		INT_MAP_DATA		0x00	
	0	ffull_int1	FIFO Full interrupt mapped to INT1	0x0	RW
	1	fwm_int1	FIFO Watermark interrupt mapped to INT1	0x0	RW
	2	drdy_int1	Data Ready interrupt mapped to INT1	0x0	RW
	3	err_int1	Error interrupt mapped to INT1	0x0	RW
	4	ffull_int2	FIFO Full interrupt mapped to INT2	0x0	RW
	5	fwm_int2	FIFO Watermark interrupt mapped to INT2	0x0	RW
	6	drdy_int2	Data Ready interrupt mapped to INT2	0x0	RW
	7	err_int2	Error interrupt mapped to INT2	0x0	RW

Register (0x59) INIT_CTRL

DESCRIPTION: Start initialization
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x59		INIT_CTRL		0x00	
	7...0	init_ctrl	Start initialization	0x0	RW

init_ctrl: Commands to start initialization

init_ctrl		
0x00	Load configuration file	Enable the mode for accept configuration file
0x01	Start initialization	Enable sensor features after loading configuration file

*Note: T*he commands should not been used more than once after POR or soft-reset, and the process of start initialization described in Chapter 2 should be followed.

Register (0x5B) INIT_ADDR_0

DESCRIPTION: Base address of the initialization data. Increment by burst write length in bytes/2 after each burst write operation. Please ignore, if your host supports to load the initialization data in a single 8kB burst write operation.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x5B		INIT_ADDR_0		0x00	
	3...0	base_0_3	Bits 0 to 3 of the base address for initialization data.	0x0	RW

Register (0x5C) INIT_ADDR_1

DESCRIPTION: Base address of the initialization data. Increment by burst write length in bytes/2 after each burst write operation. Please ignore, if your host supports to load the initialization data in a single 8kB burst write operation.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x5C		INIT_ADDR_1		0x00	
	7...0	base_11_4	Bits 4 to 11 of the base address for initialization data.	0x0	RW

Register (0x5E) INIT_DATA

DESCRIPTION: Initialization register
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x5E		INIT_DATA		0x00	
	7...0	data	Register for initialization data	0x0	RW

Register (0x5F) INTERNAL_ERROR

DESCRIPTION: Internal error flags. Value of all reserved bits should be ignored.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x5F		INTERNAL_ERROR		0x00	
	1	int_err_1	Internal error flag - long processing time, processing halted	0x0	R
	2	int_err_2	Internal error flag - fatal error, processing halted	0x0	R
	4	feat_eng_disabled	Feature engine has been disabled by host during sensor operation	0x0	R

Register (0x68) AUX_IF_TRIM

DESCRIPTION: Auxiliary interface trim register (NVM backed)
RESET: 0x01
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x68		AUX_IF_TRIM		0x01	
	1...0	asda_pupsel	Pullup configuration for ASDA **Value** **Name** **Description** 0x00 pup_res_off Pullup off 0x01 pup_res_40k Pullup 40k 0x02 pup_res_10k Pullup 10k 0x03 pup_res_2k Pullup 2k	0x1	RW

Register (0x6A) NVM_CONF

DESCRIPTION: NVM Configuration
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x6A		NVM_CONF		0x00	
	1	nvm_prog_en	Enable NVM programming. **Value** **Name** **Description** 0x00 disable disable 0x01 enable enable	0x0	RW

Register (0x6B) IF_CONF

DESCRIPTION: Serial interface settings
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x6B		IF_CONF		0x00	
	0	spi3	Configure SPI Interface Mode for primary interface **Value Name Description** 0x00 spi4 SPI 4-wire mode 0x01 spi3 SPI 3-wire mode	0x0	RW
	1	spi3_ois	Configure SPI Interface Mode for OIS interface (if enabled) **Value Name Description** 0x00 spi4 SPI 4-wire mode 0x01 spi3 SPI 3-wire mode	0x0	RW
	4	ois_en	Interface configuration - OIS enable bit. It has lower priority than aux_en.	0x0	RW
	5	aux_en	Interface configuration - AUX enable bit. It has higher priority than ois_en.	0x0	RW

Register (0x6C) DRV

DESCRIPTION: Drive strength control register (NVM backed)
RESET: 0xFF
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x6C		DRV		0xFF	
	2...0	io_pad_drv1	Output pad drive strength setting.	0x7	RW
	3	io_pad_i2c_b1	Output pad drive strength setting.	0x1	RW
	6...4	io_pad_drv2	Output pad drive strength setting.	0x7	RW
	7	io_pad_i2c_b2	Output pad drive strength setting.	0x1	RW

Register (0x6D) ACC_SELF_TEST

DESCRIPTION: Settings for the accelerometer self-test configuration and trigger
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x6D		ACC_SELF_TEST		0x00	
	0	acc_self_test_en	Enable accelerometer self-test **Value Name Description** 0x00 disabled disabled 0x01 enabled enabled	0x0	RW
	2	acc_self_test_sign	select sign of self-test excitation as **Value Name Description** 0x00 negative negative 0x01 positive positive	0x0	RW
	3	acc_self_test_amp	select amplitude of the selftest deflection: **Value Name Description** 0x00 low low 0x01 high high	0x0	RW

Register (0x6E) GYR_SELF_TEST_AXES

DESCRIPTION: Settings for the gyroscope AXES self-test configuration and trigger
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x6E		GYR_SELF_TEST_AXES		0x00	
	0	gyr_st_axes_done	STATUS: functional test of detection channels finished.	0x0	R
	1	gyr_axis_x_ok	status of gyro X-axis self test	0x0	R
	2	gyr_axis_y_ok	status of gyro Y-axis self test	0x0	R
	3	gyr_axis_z_ok	status of gyro Z-axis self test	0x0	R

Register (0x70) NV_CONF

DESCRIPTION: NVM backed configuration bits.
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x70		NV_CONF		0x00	
	0	spi_en	disable the I2C and enable SPI for the primary interface, when it is in autoconfig mode **Value** **Name** **Description** 0x00 disabled I2C enabled 0x01 enabled I2C disabled	0x0	RW
	1	i2c_wdt_sel	Select timer period for I2C Watchdog **Value** **Name** **Description** 0x00 short I2C watchdog timeout after 1.25 ms 0x01 long I2C watchdog timeout after 40 ms	0x0	RW
	2	i2c_wdt_en	I2C Watchdog at the SDA pin in I2C interface mode **Value** **Name** **Description** 0x00 Disable Disable I2C watchdog 0x01 Enable Enable I2C watchdog	0x0	RW
	3	acc_off_en	Add the offset defined in the off_acc_[xyz] OFFSET register to filtered and unfiltered Accelerometer data **Value** **Name** **Description** 0x00 disabled Disabled 0x01 enabled Enabled	0x0	RW

Register (0x71) OFFSET_0

DESCRIPTION: Offset compensation for Accelerometer X-axis (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x71		OFFSET_0		0x00	
	7...0	off_acc_x	Accelerometer offset compensation (X-axis).	0x0	RW

Register (0x72) OFFSET_1

DESCRIPTION: Offset compensation for Accelerometer Y-axis (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x72		OFFSET_1		0x00	
	7...0	off_acc_y	Accelerometer offset compensation (Y-axis).	0x0	RW

Register (0x73) OFFSET_2

DESCRIPTION: Offset compensation for Accelerometer Z-axis (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x73		OFFSET_2		0x00	
	7...0	off_acc_z	Accelerometer offset compensation (Z-axis).	0x0	RW

Register (0x74) OFFSET_3

DESCRIPTION: Offset compensation for Gyroscope X-axis (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x74		OFFSET_3		0x00	
	7...0	gyr_usr_off_x_7_0	Gyroscope offset compensation (X-axis).	0x0	RW

Register (0x75) OFFSET_4

DESCRIPTION: Offset compensation for Gyroscope Y-axis (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x75		OFFSET_4		0x00	
	7...0	gyr_usr_off_y_7_0	Gyroscope offset compensation (Y-axis).	0x0	RW

Register (0x76) OFFSET_5

DESCRIPTION: Offset compensation for Gyroscope Z-axis (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x76		OFFSET_5		0x00	
	7...0	gyr_usr_off_z_7_0	Gyroscope offset compensation (Z-axis).	0x0	RW

Register (0x77) OFFSET_6

DESCRIPTION: Offset compensation (MSBs gyroscope, enables) (NVM backed)
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x77		OFFSET_6		0x00	
	1...0	gyr_usr_off_x_9_8	Gyroscope offset compensation (X-axis).	0x0	RW
	3...2	gyr_usr_off_y_9_8	Gyroscope offset compensation (Y-axis).	0x0	RW
	5...4	gyr_usr_off_z_9_8	Gyroscope offset compensation (Z-axis).	0x0	RW
	6	gyr_off_en	Add the offset defined in the gyr_usr_off_[xyz] OFFSET register to filtered and unfiltered Gyroscope data **Value Name Description** 0x00 disabled Disabled 0x01 enabled Enabled	0x0	RW
	7	gyr_gain_en	Compensate the gain as described in section "Sensitivity Error Compensation". **Value Name Description** 0x00 disabled Disabled 0x01 enabled Enabled	0x0	RW

Register (0x7C) PWR_CONF

DESCRIPTION: Power mode configuration register
RESET: 0x03
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x7C		PWR_CONF		0x03	
	0	adv_power_save	Advanced power save disabled. **Value** **Name** **Description** 0x00 aps_off Advanced power save disabled. 0x01 aps_on Advanced power mode enabled.	0x1	RW
	1	fifo_self_wake_up	FIFO read disabled in low power mode **Value** **Name** **Description** 0x00 fsw_off FIFO read disabled in low power mode 0x01 fsw_on FIFO read enabled in low power mode after FIFO interrupt is fired	0x1	RW
	2	fup_en	Fast power up enable **Value** **Name** **Description** 0x00 fup_off Fast power up disabled 0x01 fup_on Fast power up enabled	0x0	RW

Register (0x7D) PWR_CTRL

DESCRIPTION: Power mode control register
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x7D		PWR_CTRL		0x00	
	0	aux_en	**Value** **Name** **Description** 0x00 aux_off Disables the Auxiliary sensor. 0x01 aux_on Enables the Auxiliary sensor.	0x0	RW
	1	gyr_en	**Value** **Name** **Description** 0x00 gyr_off Disables the Gyroscope. 0x01 gyr_on Enables the Gyroscope.	0x0	RW
	2	acc_en	**Value** **Name** **Description** 0x00 acc_off Disables the Accelerometer. 0x01 acc_on Enables the Accelerometer.	0x0	RW
	3	temp_en	**Value** **Name** **Description** 0x00 temp_off Disables the Temperature sensor. 0x01 temp_on Enables the Temperature sensor.	0x0	RW

Register (0x7E) CMD

DESCRIPTION: Command Register
RESET: 0x00
DEFINITION (Go to register map):

Address	Bit	Name	Description	Reset	Access
0x7E		CMD		0x00	
	7...0	cmd	Available commands (Note: Register will always return 0x00 as read result): **Value** **Name** **Description** 0xa0 nvm_prog Writes the NVM backed registers into NVM 0xb0 fifo_flush Clears FIFO content 0xb6 softreset Triggers a reset, all user configuration settings are overwritten with their default state	0x0	W

5. Legal disclaimer

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6. Document History and Modification

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