

BMI423

Small, versatile 6DoF sensor module



BMI423 Datasheet

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1 Basic Description

The BMI423 is an advanced, small, highly integrated, low power inertial measurement unit (IMU) that combines precise acceleration and angular rate (gyroscopic) measurements with intelligent on-chip motion-triggered interrupt features. The BMI423 integrates

- a 24 bit digital, triaxial accelerometer with two high-resolution ranges configurable to $\pm 8\text{ g}$ and $\pm 32\text{ g}$
- a 24 bit digital, triaxial gyroscope with high-resolution range of $\pm 4000^\circ/\text{s}$
- a 16 bit digital temperature sensor for an operating temperature range $-40^\circ\text{C} \dots +85^\circ\text{C}$

Key Features

- Compact standard size $3.00 \times 2.50\text{ mm}^2$ LGA over-mold package, 14 pins, height 0.83 mm
- Primary digital interface with up to 10 MHz SPI target (4-wire, 3-wire), 12.5 MHz I³C¹ and 1 MHz I²C (Fm+)
- Sample rates (ODR): 0.78125 Hz ... 6.4 kHz (nominal)
- Programmable low-pass filtering
- Wide power supply range: analog VDD 1.71 V ... 3.63 V and VDDIO 1.08 V ... 3.63 V, both independent
- Ultra-low current consumption: typ. 575 μA (in full ODR and aliasing-free operation)
- Built-in power management unit (PMU) for advanced power management and low power modes
 - $< 1\text{ ms}$ group delay
 - Up to 4 kB on-chip FIFO data buffer for accelerometer, gyroscope, temperature, and sensor time stamps
 - Fast offset error compensation for accelerometer and gyroscope
 - HW synchronization of accelerometer, gyroscope and temperature ($< 1\text{ }\mu\text{s}$)
 - Sensor time stamps for accurate time synchronization from device to controller ($< 40\text{ }\mu\text{s}$)
 - Two I/O pins independently programmable for detection and synchronization events usable for interrupts
 - Few times programmable non-volatile memory for persistent user configuration
- Integrated on-chip engine providing smart features for always-on applications using the IMU ultra-low power domain:
 - Motion detector
 - Step detector
 - Plug 'n' play step counter
 - Single tap, double tap, and triple tap detector
 - Voice activity detector
 - Wrist wear wake-up
 - Wrist gesture detection
- RoHS compliant, halogen and lead-free

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2 Specification

This chapter provides the specifications for the BMI423. Minimum values and maximum values are provided for standard distributed quantities as $\mu \pm 3\sigma$. Unless stated otherwise, the specifications provide the characteristics for a nominal supply voltage of $V_{DD} = V_{DDIO} = 1.8V$ either at an ambient temperature of $T_A = 25^\circ C$ or, if the characteristic is specified with respect to temperature, for the operating temperature range T_O from $-40^\circ C$ up to $+85^\circ C$.

Electrical Specifications Tables 1 and 2 provide the electrical parameters and characteristics for the device.

Table 1: Basic Electrical Parameter Specification

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage core domain	V_{DD}		1.71	1.8	3.63	V
Supply voltage I/O domain	V_{DDIO}		1.08	1.2	3.63	V
Voltage input low level	V_{IL}	SPI, I ² C & I3C			0.3 V_{DDIO}	V
Voltage input high level	V_{IH}	SPI, I ² C & I3C	0.7 V_{DDIO}			V
Voltage input hysteresis	V_{Hys}	SPI, I ² C & I3C	0.1 V_{DDIO}			V
Voltage output low level	V_{OL}	SPI			0.2 V_{DDIO}	V
Voltage output high level	V_{OH}	SPI	0.8 V_{DDIO}			V
Clock Frequency	f_{I3C}	Max. load on SDI or SDO 30pF, $V_{DDIO} \geq 1.62V$			12.5	MHz
	f_{SPI}				10	MHz
	f_{I3C}, f_{SPI}	$V_{DDIO} < 1.62V$			8	MHz
NVM write	$n_{FTP-NVM}$				100	cycles
Operating temperature	T_O		-40		+85	$^\circ C$

Table 2: Electrical Performance Specification

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current consumption	I_{DD}	A+G suspend mode		14		μA
		A _{only} low power mode, $f_{A,lp} = 25Hz$		22		
		A _{only} high performance mode, $f_{A,hp} = \max$		158		
		A+G high performance mode, $f_{A,hp} = f_{G,hp} = \max$		575		
		A+G normal mode, $f_{A,nm} = f_{G,nm} = \max$		502		
		A+G low power mode, $f_{A,lp} = f_{G,lp} = 25Hz$		315		
Power on time	Δt_{PO}	Time from supply "on" to serial I/F operational		1.2		ms

Accelerometer Specifications Tables 3, 4 and 5 provide the operating conditions for the accelerometer and the related performance and mechanical characteristics. ¹

Table 3: Operating conditions for the accelerometer

Parameter	Symbol	Condition	Min	Typ	Max	Units
Acceleration range	$a_{FS,24bit}$	Selectable via serial digital interface		± 8 ; ± 32		g
	$a_{FS,16bit}$			± 2 ; ± 4 ; ± 8 ; ± 16 ; ± 32		
Start-up time	$t_{A,SU}$	suspend to high performance mode $f_{A,hp} = \max$		2.4		ms
Accuracy of the sample rate (ODR)	$\Delta f_{A,hp,T}$	T_O , A_{only} mode, high performance mode		± 1.7		%

Table 4: Performance characteristics of the accelerometer

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution			16	24		bit
Sensitivity	$S_{A,24bit}$	$a_{FS} = 32g$		131072		$\frac{LSB}{g}$
		$a_{FS} = 8g$		1048576		
	$S_{A,16bit}$	$a_{FS} = 32g$		512		
		$a_{FS} = 16g$		2048		
		$a_{FS} = 8g$		4096		
		$a_{FS} = 4g$		8192		
		$a_{FS} = 2g$		16384		
Sensitivity error	$S_{A,err,8g}$	soldered		± 0.16		%
	$S_{A,err,8g,pq}$	soldered, over life time ¹		± 0.25		
Sensitivity error change over temperature	$\frac{\Delta S_{A,err,8g}}{\Delta T}$ (TCS _A)	T_O , best fit straight line		± 0.0015		$\frac{\%}{K}$
Zero-g offset	O_A	soldered		± 20		mg
	$O_{A,pq}$	soldered, over life time ¹		± 36		
Zero-g offset change over temperature	$\frac{\Delta O_A}{\Delta T}$ (TCO _A)	T_O , best fit straight line		± 0.25		$\frac{mg}{K}$
Noise density	$n_{A,density,8g}$	High performance mode, $a_{FS} \leq 8g$		90		$\frac{\mu g}{\sqrt{Hz}}$
Noise density	$n_{A,density,32g}$	High performance mode, $a_{FS} \geq 16g$		120		$\frac{\mu g}{\sqrt{Hz}}$
Non-linearity error	$S_{A,NL}$	best fit straight line, $a_{FS} = 8g$		± 0.2		%FS
Output data rate	$f_{A,hp}$, $f_{A,n}$	High performance and normal mode	12.5		6400	Hz
	$f_{A,lpm}$	Low-power mode	0.78125		200	

¹Life time characteristic(s) demonstrated by qualification.

Table 5: Mechanical characteristics of the accelerometer

Parameter	Symbol	Condition	Min	Typ	Max	Units
Cross axis sensitivity: Non-orthogonality	$S_{A,YX},$ $S_{A,ZX},$ $S_{A,ZY}$	Non-orthogonality among axes, evaluated as lower triangular matrix		0.15		%
Cross axis sensitivity: Alignment error	$\alpha_A, \beta_A,$ γ_A	Relative to package outline		± 0.5		°
Zero-g offset over PCB strain	$O_{A,bending}$	soldered		± 0.0175		$\frac{mg}{\mu strain}$

Gyroscope Specifications The Tables 6, 7 and 8 provide the operating conditions for the gyroscope and the corresponding performance and mechanical characteristics. ²

Table 6: Operating conditions for the gyroscope

Parameter	Symbol	Condition	Min	Typ	Max	Units
Angular rate range	$\omega_{FS,24bit}$	Selectable via serial digital interface		± 4000		$^{\circ}/s$
	$\omega_{FS,16bit}$			$\pm 125;$ $\pm 250;$ $\pm 500;$ $\pm 1000;$ $\pm 2000;$ ± 4000		
Start-up time	$t_{G,SU}$	suspend to high performance mode, $f_{G,hp} = \text{max including filter settling}$		53		ms
Accuracy of the sample rate (ODR)	$\Delta f_A =$ $\Delta f_G =$ Δf_T	Any mode with gyroscope enabled in any mode		± 0.45		%
	$\frac{\Delta f_{G,hp}}{\Delta T}$	T_O , combo mode, high performance mode		0.00275		$\frac{\%}{K}$

²Life time characteristic(s) demonstrated by qualification.

Table 7: Performance characteristics of the gyroscope

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution			16	24		bit
Sensitivity	$S_{G,24bit}$	$\omega_{FS} = 4000^{\circ}/s$		2097.152		$\frac{LSB}{^{\circ}/s}$
	$S_{G,16bit}$	$\omega_{FS} = 4000^{\circ}/s$		8.192		
		$\omega_{FS} = 2000^{\circ}/s$		16.384		
		$\omega_{FS} = 1000^{\circ}/s$		32.768		
		$\omega_{FS} = 500^{\circ}/s$		65.536		
		$\omega_{FS} = 250^{\circ}/s$		131.072		
		$\omega_{FS} = 125^{\circ}/s$		262.144		
Sensitivity error	$S_{G,err}$	soldered		± 0.3		%
	$S_{G,err,pq}$	soldered, over life time ²		± 0.4		
Sensitivity error change over temperature	$\frac{\Delta S_{G,err}}{\Delta T}$ (TCS _G)	T_O , best fit straight line		± 0.005		$\frac{\%}{K}$
Zero rate offset	$O_{G,pq}$	Soldered		± 0.5		$^{\circ}/s$
	$O_{G,pq}$	Soldered, over life time ²		± 0.6		
Zero rate offset change over temperature	$\frac{\Delta O_G}{\Delta T}$ (TCO _G)	T_O , best fit straight line		± 0.007		$\frac{^{\circ}/s}{K}$
Noise density	$n_{G,density,x/z}$	High performance mode, X-axis/Z-axis		0.0047		$\frac{^{\circ}/s}{\sqrt{Hz}}$
	$n_{G,density,y}$	High performance mode, Y-axis		0.005		
Nonlinearity error	$S_{G,NL}$	best fit straight line, $\omega_{FS} = 4000^{\circ}/s$		± 0.04		%
Output Data Rate	$f_{G,hp}, f_{G,n}$	High performance and normal mode	12.5		6400	Hz
	$f_{G,lpm}$	Low-power mode	0.78125		200	

Table 8: Mechanical characteristics of the gyroscope

Parameter	Symbol	Condition	Min	Typ	Max	Units
Cross axis sensitivity: Non-orthogonality	$S_{G,YX}, S_{G,ZX}, S_{G,ZY}$	Non-orthogonality among axes, evaluated as lower triangular matrix		± 0.1		%
Cross axis sensitivity: Alignment error	$\alpha_G, \beta_G, \gamma_G$	Relative to package outline		± 0.5		°
Zero-rate offset over PCB strain	$O_{G,bending}$	soldered		± 0.2		$\frac{^{\circ}/s}{mstrain}$
Zero rate offset error, gravitation induced	$O_{G,g}$	Gravitation (1g) parallel to each main axis		± 0.01		$^{\circ}/s$

Temperature Sensor Specifications Table 9 provides the temperature sensor related characteristics.

Table 9: Characteristics of the temperature sensor

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution				16		bits
Measurement Range	T_S		-41		87	°C
Output at 25°C				0		LSB
Sensitivity	S_T			512		$\frac{\text{LSB}}{\text{K}}$
Temperature offset	O_T	After soldering		0.6		K
Temperature sensitivity error		After soldering, T_O		2		%
Output Data Rate	$f_{T,G}, f_{T,combo}$	Any power operation mode with gyroscope in high performance mode or normal mode			50	Hz
	$f_{T,other}$	Any power operation mode with gyroscope either disabled, in low power mode or drive only enabled			25	
	$f_{T,A-only,lp}$	Accelerometer in low power mode, gyroscope disabled			12.5	

3 Absolute Maximum Ratings

Stress beyond the limits stated as “Absolute maximum ratings” in Table 10 may cause permanent damage to the product. Exposure to “Absolute maximum ratings” conditions for extended periods or multiple times may affect product reliability.

Table 10: Absolute maximum ratings

Parameter	Condition	Min	Max	Units
Voltage at Supply Pin	V_{DD} Pin	−0.3	4	V
	V_{DDIO} Pin	−0.3	4	V
Voltage at any Logic Pin	Non-Supply Pin-out	−0.3	$V_{DDIO} + 0.3$ and < 4	V
Passive Storage Temperature Range	$\leq 65\%rH$		+150	°C
OTP Non-Volatile Memory Data Retention	$T = +85\text{ °C}$	10		y
ESD	HBM at any pin JESD22-A114F (class 2)		2000	V
	CDM JESD22-C101E (class C2)		500	
	MM JESD22-A115		200	

4 Quick Start Guide

The purpose of this section is to provide developers, who want to start working with the device, with some very basic hands-on examples to get the integration into an application started. Before starting the test, the device has to be properly connected to the host and powered up. For more information about it, please find details in chapter 6 and section 8.2.

Notes on the Serial Interface Support The communication between application processor and the device will happen over one of the interfaces I3C, I²C or SPI. Regardless of the communication protocol, each register read operation includes the reading of two dummy bytes inserted before the desired payload. For more information about the interfaces and the protocol selection, see chapter 6.

The device is configured for suspend mode after Power On Reset (POR) or soft reset. In this device operation mode, reading and writing to the registers is possible without requiring to switch the operation mode of the device.

First Application Setup Example Procedures After proper power up by applying the stable supply voltage to the corresponding device pins, the device enters automatically into the POR sequence. To ensure proper use of the device, certain configuration steps from the host are a mandatory prerequisite. The most typical operations will be explained in the following application examples by sequence diagrams:

1. Test communication and initialize the device:

- a. Read the chip identifier to ensure correct communication. The default serial interface configuration is I3C and I²C. One initial dummy read configures it to SPI.

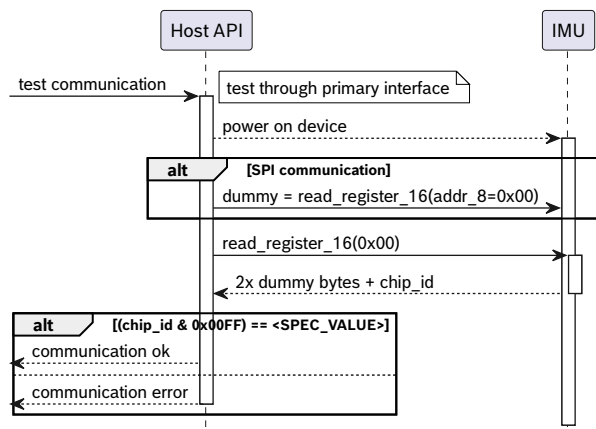


Figure 1: Device communication test

- b. Checking the correct initialization status

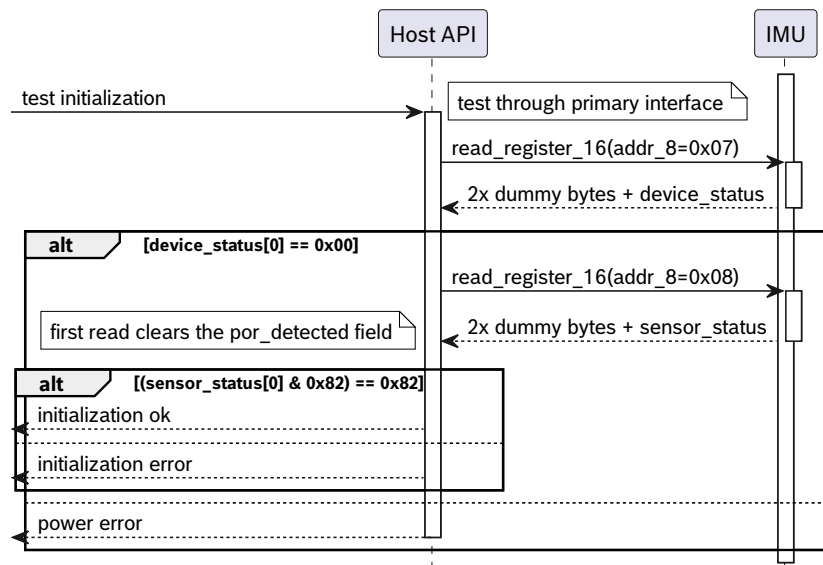


Figure 2: Device initialization status test

2. Configure the device for I3C communication:

Note: for the I3C read operation, two dummy bytes are inserted when reading from registers. For example, in order to read the chip identifier in register 0x00, in total 4 bytes must be read with a burst. The first 2 bytes are dummy bytes, the second two bytes are the chip id register word value where only the least significant byte is valid for the chip id. For more details refer to subsection 6.2.3.

About how to issue the ENTDA0(0x07) or SETDASA(0x87) command, please refer to I3C Specification. As an example, the SETDASA command shown below in Fig. 3.

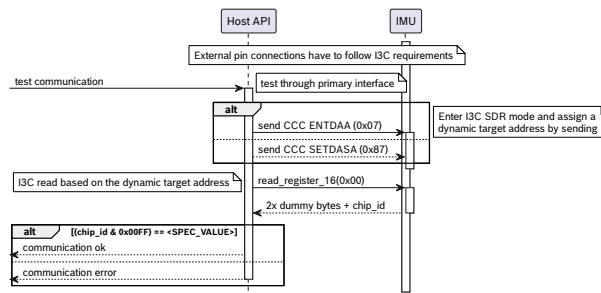


Figure 3: Configure the device for I3C communication

3. Operate the accelerometer of the device in low power mode:

Setting the data processing parameters for power, averaging and range is followed by reading sensor data. For more details refer to subsection 5.6.1.

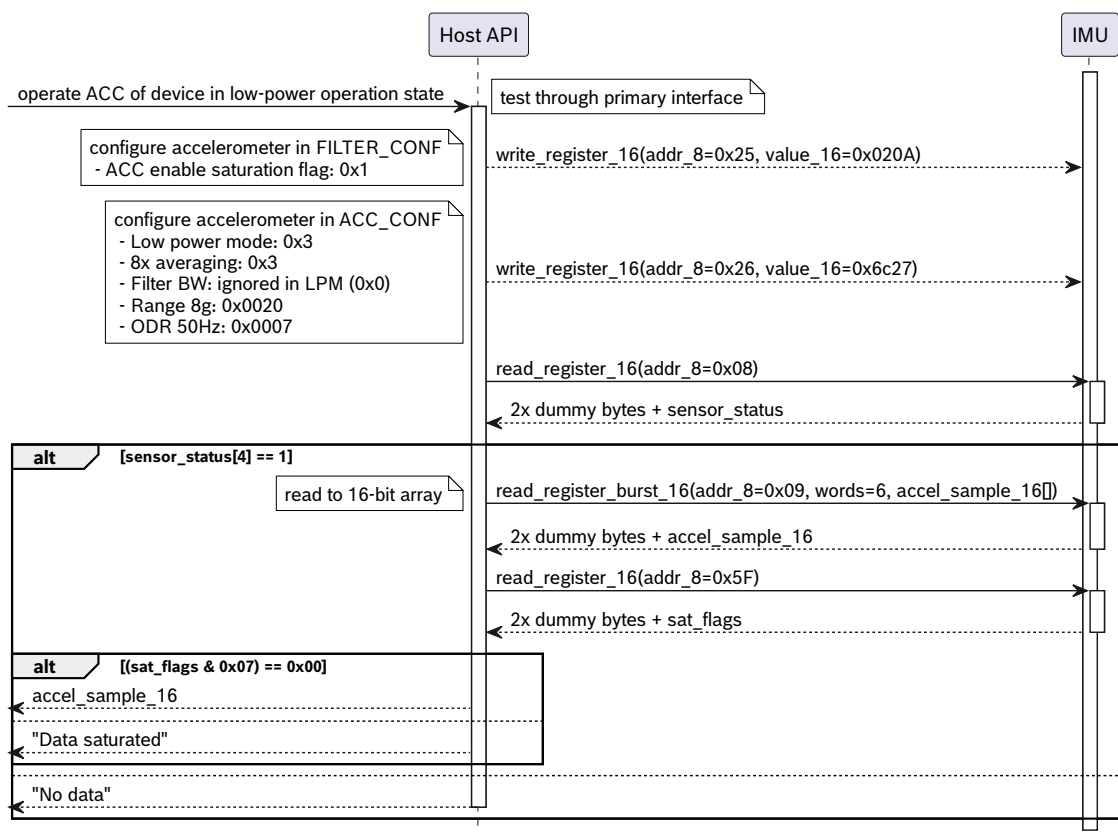


Figure 4: Configure the accelerometer in low power operation state

4. Operate the device in high performance power operation state:

Setting the data processing parameters for power, bandwidth and range followed by reading sensor data. For more details refer to subsection 5.6.1.

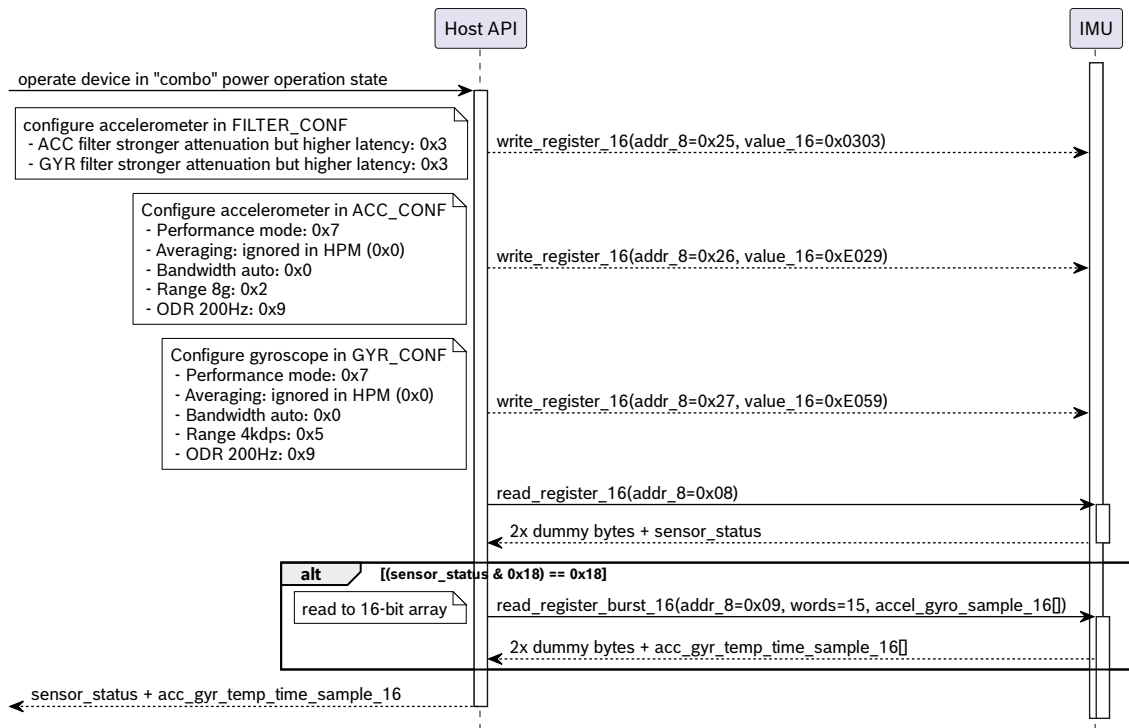


Figure 5: Configure the accelerometer and gyroscope in high performance operation state

Further Steps: These are some basic examples, and the device has many more capabilities that are described in the other chapters of this document. Those include for example FIFO data buffering, power saving, synchronization capabilities with the host processor, sample/data synchronization, etc.

Notes on the Data Protocol The host operates the device through the register map with 8-bit addressing to 16-bit data. Data is retrieved from the device by sending one address byte and then reading the required number of dummy bytes followed by two bytes for each register to be read. If only the least significant byte of an register is needed, only the first byte has to be read and the second one will be discarded automatically by the device. Data is written to the device by sending one address byte followed by two bytes for each register to be updated. Note: if only one byte is sent, the device will discard the received data and not update the targeted register. If an odd number of bytes is sent, the device will discard the last received byte and not update the last targeted register.

For more information about the data protocol and the register map including its special addresses, please refer to the chapters 7 and 6.

5 Functional Descriptions and Features

This chapter details the functions and their features with references to the data registers of the device. For a more detailed description of the registers including their addresses, partitioning, and values, please refer to chapter 7.

5.1 System Configurations

The device supports multiple configurations with its 14 pins. The simplest configuration is the device connected as target via primary interface with I3C, I2C or SPI to an application processor as shown in Figure 6.

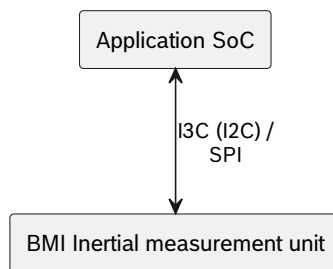


Figure 6: System Configuration

5.2 Block Diagram

Figure 7 details this logical signal view of the device from analog sensing through analog digital conversion, compensation, filtering and feature computation to the data and the protocol interfaces. The device provides sensing independent for acceleration and angular rate. The accelerometer measures the direction and magnitude of the acceleration applied to the device. In a free fall scenario, an accelerometer will report a vector of zeros. The gyroscope measures the angular rate and is reporting a vector zeros when the device is at rest. The device includes as further sensing capability a temperature sensor. All samples are reported synchronously with a unique time value.

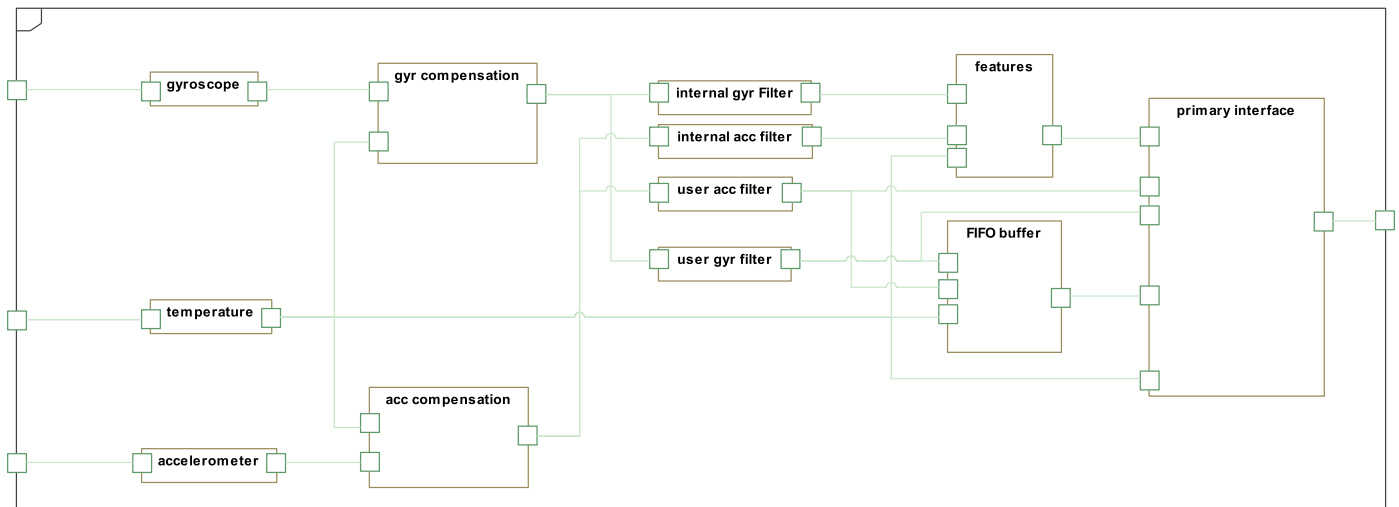


Figure 7: Block Diagram

5.3 Supply Voltage and Power Management

The device has two distinct power supplies:

- the main power supply via the VDD pin with the corresponding GND pin, and

- the IO power supply via the VDDIO pin with the corresponding GNDIO pin, driving the digital communication interface.

There are no limitations with respect to the voltage levels supplied to the VDD and VDDIO pins as long as they remain within the respective operating range, see section 6.1. Furthermore, the device can be completely switched off, that is $VDD = 0\text{ V}$, while keeping the VDDIO supply within the operating range or vice versa. If the VDDIO supply is switched off, all digital interface pins, that is CSB, SDX and SCX, must be kept close to GNDIO potential. The device is reset when the supply voltage provided to at least one of the supply pins VDD or VDDIO drops below the corresponding specified minimum values. No constraints exist for the minimum slew-rate of the voltage applied to the VDD and VDDIO pins.

5.4 Power On Reset and Device Initialization

During Power on Reset (POR), the voltages VDD and VDDIO are ramped to their respective target levels. After the supply voltages reach their target levels, registers are accessible after the start-up time. After every power on reset or soft reset, the device enters the suspend power operation mode. All registers of the device can be read and written without switching the device operation mode.

It is recommended before continuing with further operation to check the device status with the power-on-reset (POR) flag after power-on, soft-reset or in case the power supply to the device was detected to be unstable such that the device itself initiated a soft-reset. It is especially important to do this to ensure the validity of values read from the device. For the default 24 bit representation, a POR event is updated in `STATUS.por_detected`, while when using the alternative 16 bit representation, the POR event is provided at `LEG_STATUS.leg_por_detected`.

5.5 Power Operation Configuration

The main power operation modes of the device are:

- Suspend state: lowest possible power consumption with all device registers accessible at full digital interface speed, see section 6.1
- Sensing-enabled state separately configurable for accelerometer and gyroscope with
 - Duty-cycled power modes: motion sensing at lowest possible power consumption:
 - Low power mode with lower noise
 - Ultra low power mode with larger noise compared to low power mode
 - Continuous sampling power modes: motion sensing at maximum performance:
 - High performance mode with lowest possible noise
 - Normal mode with noise increased compared to high performance mode

In addition to the Suspend state, the device can be put into a Deep-Suspend state via `PWR_CONF.adv_power_save` having the lowest possible power consumption. After updating `PWR_CONF.adv_power_save` from the host, short delays have to be awaited before issuing the next read or write: 400 μs after a writing 0b1 and 100 μs after writing 0b0. In the Deep-Suspend state, the device retains its configuration and no other register access is possible except for write-access to `PWR_CONF.adv_power_save`. All read-accesses result in `CHIP_ID`. Figure 8 provides a graphical overview of the system power states and the possible transitions.

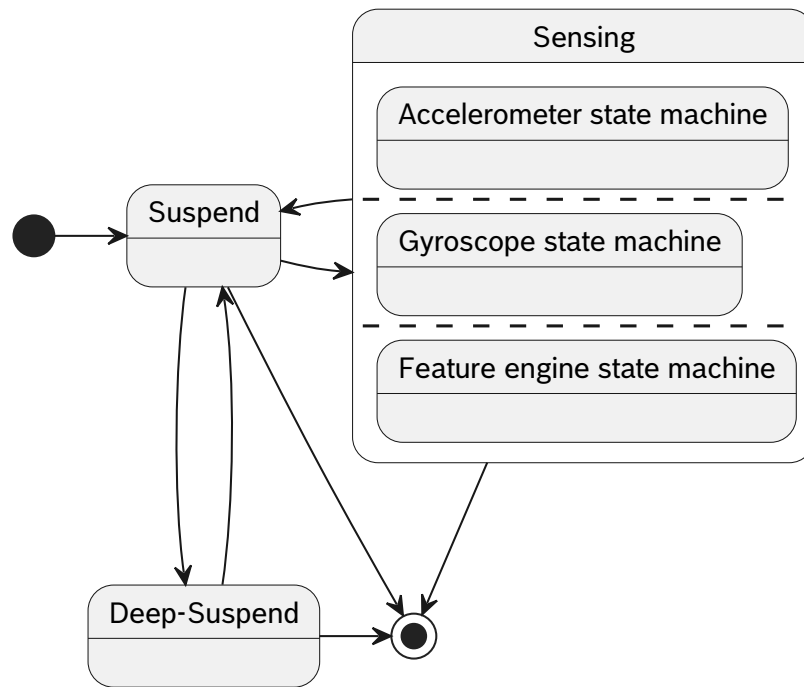


Figure 8: System power operation states

The switch among the power states Suspend versus Sensing-enabled is controlled through the configuration of the accelerometer and the gyroscope. The registers `ACC_CONF.acc_mode` and `GYR_CONF.gyr_mode` enable and disable the accelerometer and the gyroscope by directly controlling the individual power state of each sensor. The temperature sensor is automatically enabled and disabled with either the accelerometer or the gyroscope being enabled or disabled. The feature engine is enabled and disabled through `FEAT_ENG_GLOB_CTRL.feat_eng_mode`. When setting a new configuration, the start-up time of the sensor depends on the prior configuration of the sensor. The performance of the new device configuration does not depend on the prior device configuration.

After Power on Reset (POR) and soft reset, the device enters the suspend state with all sensors disabled. As next step after enabling a sensor, check before using sampled values from a sensor the availability of the corresponding sample ready (DRDY) event either by polling the corresponding register or configuring the associated events for triggering interrupt(s) on the corresponding host. In case the sample ready event is not available after the start-up time of an enabled sensor, the user should check the content of `ERR_REG.fatal_err` and, for the gyroscope, `ERR_REG.gyr_err`. For the gyroscope, the timeout until an error will be reported in `ERR_REG.gyr_err` is max 350 ms. Before enabling a sensor a user should check that no error is reported in `ERR_REG.fatal_err`.

Table 11 below shows for the sensing state the configurations required for the individual power operation modes. For reference, the table lists the numbers for the typical current consumption of selected device configurations. For the numbers related to a duty-cycled power operation mode of a sensor, averaging is always disabled.

Table 11: Power operation modes

		ACC_CONF.acc_mode	GYR_CONF.gyr_mode	PWR_CONF.adv_power_save	Typical current consumption μA ¹
Deep-Suspend mode		0b000	0b000	0b001	6
Suspend mode		0b000	0b000	0b000	14
Ultra-Low power mode	Accel only	0b010	0b000	0b000	20 ²
Low power mode	Accel only	0b011	0b000	0b000	22 ²
	Gyro only	0b000	0b011	0b000	315 ³
	IMU	0b011	0b011	0b000	315 ^{2,3}
High performance mode ⁴	Accel only	0b111	0b000	0b000	158
	Gyro only	0b000	0b111	0b000	560
	IMU	0b111	0b111	0b000	575
Normal mode ⁴	Accel only	0b100	0b000	0b000	120
	Gyro only	0b000	0b100	0b000	495
	IMU	0b100	0b100	0b000	502

5.6 Physical Sensing Features

The sensor outputs the three signals acceleration, angular rate and temperature along with the time of the device when the sensors capture the samples. A burst read on the register set of data output from the sensors always provides self contained and therefore consistent values for acceleration, angular rate, temperature and sensor time.

The documentation is structured into subsections containing information specific to the accelerometer and gyroscope, followed by one subsection providing information common to the accelerometer and gyroscope. This section is concluded at its very end with a subsection on other output signals.

5.6.1 Accelerometer

The device provides the three dimensional acceleration signal via through registers and the FIFO data buffer. The primary data output and its configuration is described in the following paragraphs and in the section 5.6.3. In the following paragraphs, the configurations for the accelerometer power operation states, measurement ranges, output sample rates and signal characteristics are explained in detail.

Accelerometer Power Operation Configuration The accelerometer is enabled according to the desired power operation setting or disabled with writing to [ACC_CONF.acc_mode](#). The accelerometer can be configured to four different power operation states, which can be grouped into duty-cycling and continuous sampling measurements:

¹Power numbers in Low power and Ultra-Low power mode are specified for ODR = 25Hz with no averaging.

²Depends on the accelerometer configuration in [ACC_CONF](#).

³Depends on the gyroscope configuration in [GYR_CONF](#).

⁴High performance power operation mode is the preferred continuous power operation mode with specification as stated in Section 2

- high performance state: continuous sampling with lowest noise,
- normal state: continuous sampling with lower power demand,
- low-power state: duty-cycled sampling with lowest noise power depending on averaging setting, and
- ultra-low-power state: duty-cycled sampling with lower power depending on averaging setting.

After power-on and soft-reset, the accelerometer is disabled by default in `ACC_CONF.acc_mode` with 0b000. Figure 9 shows the state diagram for the accelerometer, including possible transitions among them. Enabling, disabling, and changing the accelerometer configuration can affect the power operation state of the temperature sensor. More details can be found in paragraph “Temperature Sensor” in subsection 5.6.4.

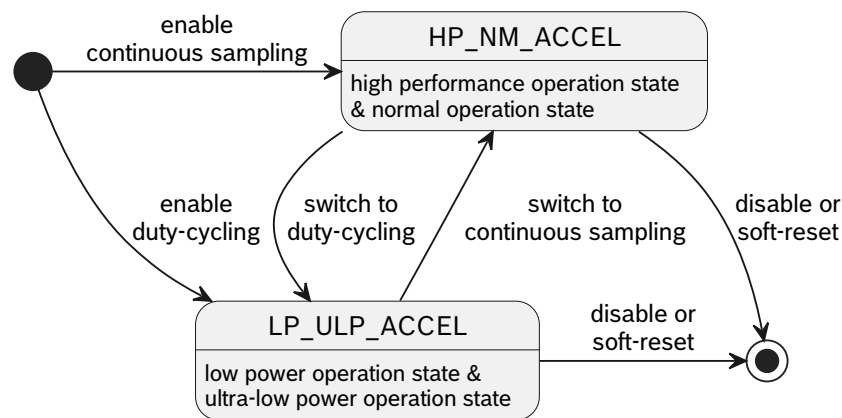


Figure 9: Accelerometer power operation states

Accelerometer Range Settings and Data Representation The configuration of the measurement range of the accelerometer depends on the selected data representation. The samples of the acceleration signal are provided in the default configuration with 24 bit data per axis. The data representation can be switched from the default representation of 24 bit to the alternative representation of 16 bit by setting `LEGACY_CONF.legacy_range_conf` to 0b1. More details are given in subsection 5.6.3.

For the default representation of 24 bit width, the range can be configured to either 8 g or 32 g, with resolutions as stated in Table 12. Due to the higher resolution, there is no necessity for further ranges, which is indicated by a yellow 'N'. The 24 bit data per axis are provided from register `ACC_DATA_X_LSB` to `ACC_DATA_Z_MSB` as 32 bit sign extended two's complement value. Each axis is split into 2 adjacent 16 bit registers of least significant word (LSW) and most significant word (MSW) with values ranging from 0xFF80'0001 to 0x007F'FFFF. Reading byte-wise the 24 bit acceleration data from the two 16 bit registers always starts with the least significant byte (LSB) up to the most significant byte (MSB). In case no valid sample is present, the reset value of 0xFF80'0000 is provided.

When the alternative representation of 16 bit is enabled, the configurable measurement ranges are 2 g, 4 g, 8 g, 16 g, and 32 g, with resolutions as stated in Table 12. In the 16 bit representation mode, the data of each axis is provided within one single 16 bit value in two's complement from register `LEG_ACC_DATA_X` to `LEG_ACC_DATA_Z`. Reading byte-wise the 16 bit acceleration data registers always returns first the LSB, then the MSB. The default value in case of invalid data is 0x8000.

After power up and soft reset, the default range is 8 g, independent of the selected data representation.

The device can be configured to detect saturation in the accelerometer signal path by writing 0b1 to `FILTER_CONF.acc_sat_flag_en`. If activated, the device detects an overflow at the input to the filters that might be not observable in the output due to the filtering. The saturation is reported for each axis individually with `SAT_FLAGS.satf_acc_x`, `SAT_FLAGS.satf_acc_y`, and `SAT_FLAGS.satf_acc_z`, but may be only interpreted if the detection is enabled. In 24 bit data representation, the status of the saturation flags is additionally available in bit 0 (LSB) of the accelerometer data. The saturation flag configuration becomes effective only when writing first to `FILTER_CONF` and afterwards write to the register `ACC_CONF`. The purpose of the saturation detection is to indicate that a saturated measurement sample was included into the filtering and may effect the output value.

The accelerometer axis orientation with respect to the device package, as shown in Figure 41, can be re-mapped from default to a user-defined orientation. The re-assignment of the axis is described in detail in section 5.11.2.

Table 12: Accelerometer resolutions per range and data representation

Measurement range	Resolution [$\mu\text{g}/\text{LSB}$] per data representation	
	24 bit	16 bit
2 g	'N'	61.035
4 g	'N'	122.07
8 g	0.954	244.141
16 g	'N'	488.282
32 g	7.629	1953.13

Accelerometer Signal Processing with Continuous Sampling The device supports the two continuous sampling power operation states “high performance” (HPM) and “normal” (NM). These can be enabled by setting `ACC_CONF.acc_mode` to 0b111 for high performance and 0b100 for normal, respectively. The sample rate output by the device (ODR) for a continuous power operation state is configured through `ACC_CONF.acc_odr` with rates ranging from 12.5 Hz up to 6400 Hz. Sample rates less than 12.5 Hz are only supported in one of the duty cycled power operation states, see the paragraph below. The acceleration samples are output continuously at equidistant time points corresponding to the time constant of the accelerometer sample rate in `ACC_CONF.acc_odr` with respect to the device clock.

Low-Pass filtering of the acceleration signal can be configured through `ACC_CONF.acc_bw` with possible combinations as shown in Table 15 and dependency on the filter characteristics configured in `FILTER_CONF.acc_filter_type`. The effects of these settings are common to the gyroscope and explained in more detail in subsection 5.6.3. The accelerometer related filter configuration becomes effective only when writing first the filter configuration to `FILTER_CONF` and then directly afterwards the register `ACC_CONF`.

The device allows a filtering of the acceleration by a configurable IIR filter. The selectable combinations of sample rates (ODR) and filter bandwidths (BW) are stated in the Table 15. Other nominal bandwidths can be selected explicitly by writing the necessary configuration value to a supported BW-ODR combination. Non-selectable BW-ODR combinations are marked with a yellow 'N'.

Note: `ACC_CONF.acc_avg_num` has no effect in continuous sampling and is used for duty-cycled output only.

Note: the filter settings have no effect when Timing Control Synchronous of I3C is enabled.

Accelerometer Signal Processing with Duty-Cycled Output Two sampling power operation states with duty cycled signal processing are available with the options “low-power” (LPM) and “ultra-low-power” (ULPM). These configurations can be enabled by setting `ACC_CONF.acc_mode` to 0b011 for low-power and 0b010 for ultra-low-power operation. The data processing can be tailored to the application and context to balance power consumption and signal noise with the number of averaging configured through `ACC_CONF.acc_avg_num` before outputting data. The sample rate of the signal available to the host (ODR) can be configured from 0.78 Hz up to 200 Hz through `ACC_CONF.acc_odr`. Valid combinations of `AVG_NUM` and ODR are given in Table 16. Sample rates greater than 200 Hz are only supported with continuous sampling power operation states.

Note: `FILTER_CONF.acc_filter_type` has no effect for duty-cycled output and is used only with continuous sampling.

Accelerometer Sample Ready Notification The controller can be notified about the availability of a new set of sampled data from the accelerometer by hardware events. Notification by an interrupt allows a low latency read of data from the controller side. Events can be forwarded to the host through one of the two (physical) interrupt pins or the in-band-interrupt (IBI) feature of I3C. To enable the data ready interrupt, it has to be mapped via `INT_MAP_HW.acc_drdy_int_map` to the desired interrupt interface with 0b01 to the INT1 pin, 0b10 to the INT2 pin or 0b11 to the I3C-IBI. The configuration of the event signaling is elaborated in more detail in section 5.9.

Instead of using the sample ready event, the event status can be determined by polling the data ready status of the accelerometer. For the default 24 bit representation, the status of the sample ready event is updated in `STATUS.drdy_acc` while when using the alternative 16 bit representation, the sample ready event is provided at `LEG_STATUS.leg_drdy_acc`. Polling has the disadvantage of non-deterministic delays caused by the different clock sources of this device and the controller side.

5.6.2 Gyroscope

The device provides the three dimensional angular rate signal via through registers and the FIFO data buffer. The primary data output and its configuration is described in the following paragraphs and in the section 5.6.3. In the following paragraphs, the configurations for the gyroscope power operation states, measurement ranges, output sample rates and signal characteristics are explained in detail.

Gyroscope Power Operation Configuration The gyroscope is enabled according to the desired power operation setting or disabled with writing to `GYR_CONF.gyr_mode`. The gyroscope can be configured to four different power operation states, which can be grouped into duty-cycling and continuous sampling measurements:

- high performance state: continuous sampling with lowest noise,
- normal state: continuous sampling with lower power demand,
- low-power state: duty-cycled sampling with lowest noise power depending on averaging setting, and
- drive-only state: no sampling, gyroscope drive still running for faster startup time.

After power-on and soft-reset, the gyroscope is disabled by default in `GYR_CONF.gyr_mode` with 0b000. Figure 10 shows the state diagram for the gyroscope, including possible transitions among them. Enabling, disabling and changing the gyroscope configuration can affect the power operation state of the temperature sensor. More details can be found in Paragraph “Temperature Sensor” in subsection 5.6.4.

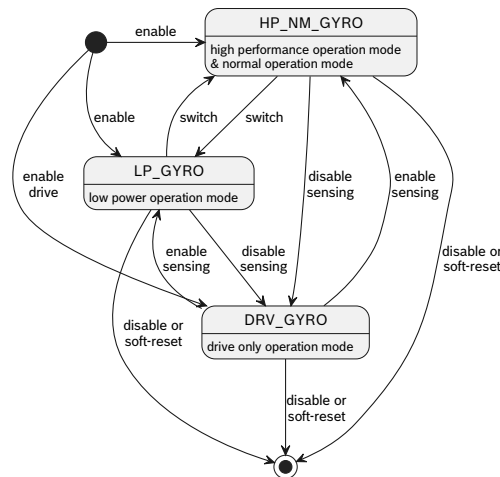


Figure 10: Gyroscope power operation states

Gyroscope Range Settings and Data Representation The configuration of the measurement range of the gyroscope depends on the selected data representation. The samples of the angular rate signal are provided in the default configuration with 24 bit data per axis. The data representation can be switched from the default representation of 24 bit to the alternative representation of 16 bit by setting `LEGACY_CONF.legacy_range_conf` to 0b1. More details are given in subsection 5.6.3.

For the default representation of 24 bit width, the range is 4000 °/s, with resolutions as stated in Table 13. Due to the higher resolution, there is no necessity for further ranges, which is indicated by a yellow 'N'. The 24 bit data per axis are provided from register `GYR_DATA_X_LSB` to `GYR_DATA_Z_MSB` as 32 bit sign extended two's complement value. Each axis is split into 2 adjacent 16 bit registers of least significant word (LSW) and most significant word (MSW) with values ranging from 0xFF80'0001 to 0x007F'FFFF. Reading byte-wise the 24 bit angular rate data from the two 16 bit registers always starts with the least significant byte (LSB) up to the most significant byte (MSB). In case no valid sample is present, the reset value of 0xFF80'0000 is provided.

When the alternative representation of 16 bit is enabled, the configurable measurement ranges are 125 °/s, 250 °/s, 500 °/s, 1000 °/s, 2000 °/s. and 4000 °/s, with resolutions as stated in Table 13. In the 16 bit representation mode, the data of each axis is provided within one single 16 bit value in two's complement from register `LEG_GYR_DATA_X` to `LEG_GYR_DATA_Z`. Reading byte-wise the 16 bit angular rate data registers always returns first the LSB, then the MSB. The default value in

case of invalid data is 0x8000.

After power up and soft reset, the default range is 4000 °/s, independent of the selected data representation.

The device can be configured to detect saturation in the gyroscope signal path by writing 0b1 to `FILTER_CONF.gyr_sat_flag_en`. If activated, the device detects an overflow at the input to the filters that might be not observable in the output due to the filtering. The saturation is reported for each axis individually with `SAT_FLAGS.satf_gyr_x`, `SAT_FLAGS.satf_gyr_y`, and `SAT_FLAGS.satf_gyr_z`, but may be only interpreted if the detection is enabled. In 24 bit data representation, the status of the saturation flags is additionally available in bit 0 (LSB) of the gyroscope data. The saturation flag configuration becomes effective only when writing first to `FILTER_CONF` and afterwards write to the register `GYR_CONF`. The purpose of the saturation detection is to indicate that a saturated measurement sample was included into the filtering and may effect the output value.

The gyroscope axis orientation with respect to the device package, as shown in Figure 41, can be re-mapped from default to a user-defined orientation. The re-assignment of the axis is described in detail in section 5.11.2.

Table 13: Gyroscope resolutions per range and data representation

Measurement range	Resolution [$m^{\circ}/s/LSB$] per data representation	
	24 bit	16 bit
125 °/s	'N'	3.815
250 °/s	'N'	7.629
500 °/s	'N'	15.259
1000 °/s	'N'	30.518
2000 °/s	'N'	61.035
4000 °/s	0.477	122.07

Gyroscope Signal Processing with Continuous Sampling The device supports the two continuous sampling power operation states “high performance” (HPM) and “normal” (NM). These can be enabled by setting `GYR_CONF.gyr_mode` to 0b111 for high performance and 0b100 for normal, respectively. The sample rate output by the device (ODR) for a continuous power operation state is configured through `GYR_CONF.gyr_odr` with rates ranging from 12.5 Hz up to 6400 Hz. Sample rates less than 12.5 Hz are only supported in one of the duty cycled power operation states, see the paragraph below. The angular rate samples are output continuously at equidistant time points corresponding to the time constant of the gyroscope sample rate in `GYR_CONF.gyr_odr` with respect to the device clock.

Low-Pass filtering of the angular rate signal can be configured through `GYR_CONF.gyr_bw` with possible combinations as shown in Table 15 and dependency on the filter characteristics configured in `FILTER_CONF.gyr_filter_type`. The effects of these settings are common to the gyroscope and explained in more detail in subsection 5.6.3. The gyroscope related filter configuration becomes effective only when writing first the filter configuration to `FILTER_CONF` and then directly afterwards the register `GYR_CONF`.

The device allows a filtering of the angular rate by a configurable IIR filter. The selectable combinations of sample rates (ODR) and filter bandwidths (BW) are stated in the Table 15. The automatically selected nominal bandwidth for a selected sample rate is marked with bold text. Other nominal bandwidths can be selected explicitly by writing the necessary configuration value to a supported BW-ODR combination. Non-selectable BW-ODR combinations are marked with a yellow 'N'.

Note: `GYR_CONF.gyr_avg_num` has no effect in continuous sampling and is used for duty-cycled output only.

Note: the filter settings have no effect when Timing Control Synchronous of I3C is enabled.

Gyroscope Signal Processing with Duty-Cycled Output One sampling power operation states with duty cycled signal processing is available with the options “low-power” (LPM). This configurations can be enabled by setting `GYR_CONF.gyr_mode` to 0b011 for low-power operation. The data processing can be tailored to the application and context to balance power consumption and signal noise with the number of averaging configured through `GYR_CONF.gyr_avg_num` before outputting data. The sample rate of the signal available to the host (ODR) can be configured from 0.78 Hz up to 200 Hz through `GYR_CONF.gyr_odr`. Valid combinations of AVG_NUM and ODR are given in Table 16. Sample rates greater than 200 Hz are only supported with continuous sampling power operation states. Table 14 states the recommended

combinations with best user experience in terms of resulting noise power vs sample rates depending on the configured averaging.

Table 14: Duty-cycled Gyroscope Sampling: Recommended Averaging Balancing Noise Power vs Current Consumption

ODR [Hz]	≤ 12.5	25	50	100	200
Number of Averages	1	8, 16, 32, 64	8; 16; 32	8; 16	8

Note: `FILTER_CONF.gyr_filter_type` has no effect for duty-cycled output and is used only with continuous sampling.

Gyroscope Sample Ready Notification The controller can be notified about the availability of a new set of sampled data from the gyroscope by hardware events. Notification by an interrupt allows a low latency read of data from the controller side. Events can be forwarded to the host through one of the two (physical) interrupt pins or the in-band-interrupt (IBI) feature of I3C. To enable the data ready interrupt, it has to be mapped via `INT_MAP_HW.gyr_drdy_int_map` to the desired interrupt interface with 0b01 to the INT1 pin, 0b10 to the INT2 pin or 0b11 to the I3C-IBI. The configuration of the event signaling is elaborated in more detail in section 5.9.

Instead of using the sample ready event, the event status can be determined by polling the data ready status of the gyroscope. For the default 24 bit representation, the status of the sample ready event is updated in `STATUS.drdy_gyr` while when using the alternative 16 bit representation, the sample ready event is provided at `LEG_STATUS.leg_drdy_gyr`. Polling has the disadvantage of non-deterministic delays caused by the different clock sources of this device and the controller side.

5.6.3 Accelerometer and Gyroscope Commons

In the following, the configuration options available for both the accelerometer and gyroscope with their effects are detailed for the individual operation states.

Continuous Signal Sampling Continuous sampling provides the highest possible signal quality for the output signals of the accelerometer and gyroscope. One can balance the latency of the samples output to the host with respect to the signal to noise power ratio (SNR) via the selection of the output sample rate (ODR) and the applied filtering option. Sample rates (ODR) supported for the accelerometer and gyroscope by continuous signal sampling range from 12.5 Hz to 6.4 kHz. Filtering options consist of selectable bandwidth and low-pass filter slopes for adjustable noise suppression capability. The filter slope can be selected for the accelerometer and gyroscope through `FILTER_CONF.acc_filter_type5` and `FILTER_CONF.gyr_filter_type5`, respectively. The available configuration options for the low-pass filter are the roll-off factors of -20 dB/dec, -40 dB/dec and -60 dB/dec. By default, the low-pass filter in the device is set to the roll-off -40 dB/dec. Table 15 provides the overview of allowed bandwidths for the selectable sample rates. The automatically selected bandwidth for a sample rate (ODR) is marked with a bold blue 'auto-sel', the other valid possibilities with a blue 'Y' and non-selectable bandwidths with a yellow 'N'. In case multiple filter configurations are allowed, the bandwidth of the low-pass filter can be switched from the automatically selected bandwidth to different settings with reduced bandwidth via `ACC_CONF.acc_bw` and `GYR_CONF.gyr_bw`. If multiple bandwidths are possible, the automatically selected bandwidth is always the largest one. In case an invalid combination is selected for the accelerometer or the gyroscope, an error is reported in `ERR_REG.acc_conf_err` or `ERR_REG.gyr_conf_err`, respectively, and no data is output. For the alternative configuration of the auto operation mode switch, configurations can be applied analogously to `ALT_FILTER_CONF.alt_acc_filter_type6` and `ALT_FILTER_CONF.alt_gyr_filter_type6`, see section 5.10.

⁵Changes to accelerometer or gyroscope specific settings in `FILTER_CONF` take effect only when first the register `FILTER_CONF` is written and afterwards either the corresponding sensor configuration register `ACC_CONF` or `GYR_CONF`.

⁶Changes to accelerometer or gyroscope specific settings in `ALT_FILTER_CONF` only take effect when first the register `ALT_FILTER_CONF` is written and subsequently either the corresponding sensor configuration register `ALT_ACC_CONF` or `ALT_GYR_CONF`.

Table 15: Filter Configuration in Continuous Power Operation States

Sample rate (ODR) [Hz]	Bandwidth [Hz]							
	800	400	200	100	50	25	12.5	6.25
6400	auto-sel	Y	Y	N	N	N	N	N
3200	auto-sel	Y	Y	Y	N	N	N	N
1600	auto-sel	Y	Y	Y	Y	N	N	N
800	N	auto-sel	Y	Y	Y	Y	N	N
400	N	N	auto-sel	Y	Y	Y	N	N
200	N	N	N	auto-sel	Y	Y	N	N
100	N	N	N	N	auto-sel	Y	N	N
50	N	N	N	N	N	auto-sel	N	N
25	N	N	N	N	N	N	auto-sel	N
12.5	N	N	N	N	N	N	N	auto-sel

Additionally, to output data without low-pass filtering, the 'bypass' option can be selected for a sample rate (ODR) of 6.4 kHz. However, lower sample rates are not supported for this case.

Note: averaging configurations have no effect in continuous sampling and are only in used for duty-cycled output.

Duty-cycled Signal Sampling Duty-cycled sampling of acceleration and angular rate is the choice to minimize the power consumption of the digitization. In power operation states with duty-cycled sampling of the acceleration and angular rate, the digitization of the signal alternates between the idle phase, where no measurements are performed, and the active phase, where data is acquired. The output to the host is the average of all samples acquired during the active phase. The number of averaged samples is configured through `ACC_CONF.acc_avg_num` and `GYR_CONF.gyr_avg_num`, respectively. A larger number of averaged samples will result in a lower noise level of the signal. As the active phase is increased, the power consumption rises. The period for changing between active and idle mode, also known as duty-cycle period, is determined automatically by the device by the value configured for the accelerometer through `ACC_CONF.acc_odr` and `ACC_CONF.acc_avg_num` and for the gyroscope through `GYR_CONF.gyr_odr` and `GYR_CONF.gyr_avg_num`, respectively. Valid combinations for these two configurations are stated in Table 16. In case of an invalid configuration, the error condition is reported in `ERR_REG.acc_conf_err` or `ERR_REG.gyr_conf_err` for the accelerometer and gyroscope, respectively, and no data will be output. For the alternative configuration of the auto operation mode switch, configurations can be applied in an analogous manner to `ACC_CONF.acc_avg_num` and `GYR_CONF.gyr_avg_num`, see section 5.10.

Note: these averaging settings have no effect in continuous sampling mode or when Synchronous Time Control of I3C is enabled. Filter configurations of bypass, 1st order, 2nd order or 3rd order filtering have no effect for duty-cycled output and are used only with continuous sampling.

Table 16: Duty-cycled Sampling: Allowed Averaging Combinations

ODR [Hz]	Averaging Configuration			
	64	32	16	8, 4, 2, 1
≥ 400	N	N	N	N
200	N	N	N	Y
100	N	Y	Y	Y
≤ 50	Y	Y	Y	Y

Configuration Change Activation The update of the device configuration contained in the registers `FILTER_CONF`, `ACC_CONF` and `GYR_CONF` takes immediate effect when no sensor is activated. In case the configuration is altered while the sensors are enabled, the changes are synchronized in with a period of 1/25.6 kHz. There will be no data output from the point of re-configuration on until the first sample of the new configuration is output.

It is recommended to merge and perform the configuration of accelerometer as well as gyroscope affecting any of power operation state, measurement range, sample rate (ODR), bandwidth or averaging, filter configuration and saturation flags

in one batch write. As described in the sections 5.6.1 and 5.6.2, the configurations for `FILTER_CONF` have to be written prior to the configurations in `ACC_CONF` and `GYR_CONF`.

16 bit Representation It is possible to switch from the default 24 bit representation to the 16 bit representation of predecessor generations. In this configuration, the data of the accelerometer and gyroscope is provided with 16 bit per axis in one single register instead of being spread over two registers. Also the data of accelerometer and gyroscope in the FIFO data buffer are stored with 16 bit per axis, further information like FIFO frame structure for 16bit representation can be found in [16 bit Representation](#). Additionally, more selectable ranges are offered due to the reduced resolution capability of the 16bit representation, see Table 12 and Table 13. This configuration for 16 bit representation can only be set after power-up of the device by writing 0b1 to `LEGACY_CONF.legacy_range_conf` and affects acceleration and angular rate output at the same time. The 16 bit representation must always be re-enabled after a soft-reset or power-on-reset.

Data Integrity The device allows reading consistent sets sample of acceleration, angular rate, temperature, sensor time, error and status information and event information of sensor signals and composite events. This is necessary, because a new set of samples could be written to the registers while a read from the registers is in progress. The integrity of this set of data is provided by a shadowing of the data in the registers `ERR_REG` to `INT_STATUS_INT2` once the read from the device commenced from one of these registers and delaying the update until the read from the registers is completed. The shadowing is also working for the 16 bit data representation when reading from the registers `LEG_ERR_REG` to `LEG_STATUS`.

5.6.4 Further Sensor Data

Temperature Sensor The values of sampled signal from the temperature sensor are provided with 16 bit in two's complement representation in the 16 bit wide register `TEMP_DATA.temperature`. Reading byte-wise the 16 bit data registers always returns first the least significant byte, then the most significant byte. When the alternative representation of 16 bit is enabled, the samples are provided in the same format in the 16 bit wide register `LEG_TEMP_DATA.leg_temperature` instead. The range of the temperature values is from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, for conversion details see register description. The temperature sensor is automatically enabled with enabling either the accelerometer or the gyroscope. It is automatically disabled when both accelerometer and gyroscope are being disabled. The register contains the invalid value 0x8000 until the first temperature measurement is completed. The sample rate (ODR) of data available to the host depends on the enabled sensors and their respective power operation state, see Table 17.

Table 17: Effective Temperature Sensor Sample rate f_T

Sensor Power Operation State Condition	Min	Typ	Max	Unit
Accelerometer in high performance mode or normal mode and gyroscope disabled or in fast start-up mode	25		25	Hz
Accelerometer in low power mode and gyroscope disabled or in fast start-up mode	$f_{A,low-power}$		12.5	
Gyroscope in high performance mode or normal mode and accelerometer disabled	50	...	50	
Gyroscope in low power mode and accelerometer disabled	$f_{G,low-power}$		12.5	
Accelerometer and gyroscope in any of high performance mode or normal mode	50	...	50	
Accelerometer in low power mode and gyroscope in high performance mode or normal mode	50	...	50	
Gyroscope in low power mode and accelerometer in high performance mode or normal mode	25		25	
Accelerometer in low power mode and gyroscope in low power mode	$\max \{f_{A,low-power}, f_{G,low-power}\}$		12.5	

Sensor Time The device provides the time of the sensors synchronized to any sample acquired from the accelerometer, gyroscope and temperature sensor. The value of the timer is provided with 24 bits width in two registers where the most significant word is stored in [SENSORTIME_DATA_MSB](#) and the least significant word in [SENSORTIME_DATA_LSB](#). The minimum increment of the timer is 39.0625 μ s per LSB of [SENSORTIME_DATA_LSB](#). A burst read on the registers always provides self contained and therefore consistent values. The sensor time will wrap around after approximately 10 minutes and approximately 55 seconds. Table 18 details the resolution and update rate of the bits in the sensor time register.

Table 18: Resolution and Update Rate of the Sensor Time

Bit <i>m</i> in SENSORTIME_DATA_MSB	23	22	21	20	19	18	17	16
Resolution [s]	327.68	163.84	81.92	40.96	20.48	10.24	5.12	2.56
Sample Rate [Hz]	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Bit <i>m</i> in SENSORTIME_DATA_LSB	15	14	13	12	11	10	9	8
Resolution [ms]	1280	640	320	160	80	40	20	10
Sample Rate [Hz]	0.78125	1.5625	3.125	6.25	12.5	25	50	100
Bit <i>m</i> in SENSORTIME_DATA_LSB	7	6	5	4	3	2	1	0
Resolution [μ s]	5000	2500	1250	625	312.5	156.25	78.125	39.0625
Sample Rate [Hz]	200	400	800	1600	3200	6400	n/a	n/a

When the alternative representation of 16 bit is enabled, the sensor time is provided analogous with 24 bit in the two registers [LEG_SENSORTIME_DATA_MSB](#) and [LEG_SENSORTIME_DATA_LSB](#) with the same representation and resolution.

The source for the sensor time varies from device to device because each device has an own oscillator. It is possible to compute and thereby compensate this device to device variation of the sample rate (ODR) compared to the nominal sample rate. By applying the value $r_{f,deviation}$ in LSB of the sample rate deviation in [IO_ODR_DEVIATION.odr_deviation](#), the relation of the device sample rate (ODR) to the nominal frequency reads

$$f_{device} = f_{nominal} \cdot \left(1 + \frac{0.0135 \cdot r_{f,deviation}}{2^4} \right) . \quad (5.1)$$

With the inverse relationship of the sample rate (ODR) to the sampling time, the sensor time can be converted similarly from the device time domain to the host time domain.

5.7 FIFO Data Buffering

The FIFO data buffer collects and stores data from selected sensors to allow a reduced number up to a minimization of data transfers between device and host. The device supports the following FIFO operating modes for the FIFO data buffer:

- Streaming mode:
 - Behavior: overwrite oldest data on buffer full condition
 - Configuration: set [FIFO_CONF.fifo_stop_on_full](#) to 0b0
- Stop-on-full mode:
 - Behavior: discard newest data on buffer full condition
 - Configuration: set [FIFO_CONF.fifo_stop_on_full](#) to 0b1

The FIFO data buffer has a size of 4096 bytes. It can trigger interrupts to the host for the conditions of FIFO data buffer filled and FIFO data buffer watermark level reached, see details in section 5.7.3. The FIFO data buffer can be configured to store

- acceleration data from the accelerometer with [FIFO_CONF.fifo_acc_en](#)=0b1,
- angular rate data from the gyroscope with [FIFO_CONF.fifo_gyr_en](#)=0b1,
- temperature data with [FIFO_CONF.fifo_temp_en](#) set to 0b1, and
- sensor time with [FIFO_CONF.fifo_sensor_time](#) set to 0b10.

The FIFO data buffer may be enabled for data acquisition in all power operation states of the device through [FIFO_CONF.fifo_en](#). Except for deep suspend mode, reading the FIFO data buffer from the controller is possible in all power operation

modes of the device.

5.7.1 Frames

Data is stored in the FIFO data buffer with frames. Each frame has a 1-byte header that indicates which data is contained in a particular frame, see Table 24. The total width of a frame stored in the buffer depends on the signal sources enabled for buffering. The total width of a frame in bytes is always an even number. Once the sources to be buffered are set, the frame width remains constant unless the configuration for sources to be stored in the data buffer is altered. Each source adds its own specific width and is placed according to a predefined ordering to a frame, see Table 19. A lower ordering number of a source means its data appears prior in a buffer frame compared to a higher ordering number of a source. With the exception of the sensor time, disabled sources do not consume space in the buffer frame. Even when the sensor time is disabled, the LSB of the sensor time is added to serve as a padding byte to ensure an even number of bytes in a frame. Any change in the FIFO configuration causing a buffer frame width to change causes an instant flush of the FIFO data buffer and, subsequently, a restart of storing data in the buffer with the new settings, see details in subsection 5.7.4.

Table 19: Order and size of sources to the FIFO data buffer

Order	Source	Size [bytes]	Description
0	FIFO buffer	1	Header of the FIFO data buffer
1	Oscillator	3 (1)	Sensortime, 24 bit, (if disabled, LSB acts as padding byte)
2	Temperature sensor	2	Temperature as 16 bit value
3	Accelerometer	10	Acceleration, 24 bit per axis (x, y, z) and one padding byte
4	Gyroscope	10	Angular rate, 24 bit per axis (x, y, z) and one padding byte

The data format in a data buffer frame is summarized in Table 20.

Table 20: FIFO Data Description

Frame Field	FIFO Data Description
Header	Enabled and update information, see Table 24
Sensor time	Same resolution as sensor time, see subsection 5.6.4
Accelerometer	Resolution as configured in ACC_CONF.acc_range , see subsection 5.6.1
Gyroscope	Resolution as configured in GYR_CONF.gyr_range , see subsection 5.6.2
Temperature	For scaling see TEMP_DATA.temperature , more details in subsection 5.6.4

Example If gyroscope, sensortime, and acceleration are enabled, then the order within the buffer frame is (header:time:acceleration:angularrate).

A change of the configuration of a sensor used as signal source, e.g. measurement range, sample rate (ODR), etc, will restart the signal processing in the device causing invalid data until the settling of the signal processing chain is completed. Invalid data is not inserted into the buffer frames and skipped automatically. Instead, during this time the header indicates 0b0 for the respective data source and, in order to keep the width of a frame constant, the reset value of the respective data source is inserted as shown in Table 21.

The combination of reset value and 0b0 in the header for a specific source can also be used to distinguish between frames with old and new settings in place. In case an inactive signal source is configured for FIFO data buffering, the value 0b0 and the reset value are placed in the header and for the frames, respectively.

Table 21: Data reset values in the FIFO data buffer

Source	Reset Value
Accelerometer	0xFF80 0000
Gyroscope	0xFF80 0000
Temperature	0x8000

16 bit Representation Overall the FIFO data buffer behaves exactly the same in 16 bit representation. Only the frame composition is adapted for the 16 bit data width compared to 24 bit standard data width, leading to the sizes for the respective sources as shown in 22. Along the frame size, also the reset values are adopted from 16 bit data output registers, to the values shown in Table 23.

Table 22: Order and size of sources to the FIFO data buffer

Order	Source	Size [bytes]	Description
0	FIFO buffer	1	FIFO data buffer header
1	Oscillator	3 (1)	Sensor time, 24 bit, (if disabled, LSB acts as padding byte)
2	Temperature sensor	2	Temperature as 16 bit value
3	Accelerometer	6	Acceleration, 16 bit per axis (x, y, z)
4	Gyroscope	6	Angular rate, 16 bit per axis (x, y, z)

Table 23: Data reset values in the FIFO data buffer Legacy-Mode

Source	Reset Value
Accelerometer	0x8000
Gyroscope	0x8000
Temperature	0x8000

5.7.2 Conditions and Details

Enabling and Disabling of the FIFO Data Buffer The FIFO data buffer may be enabled in any sequence with respect to the enabling of sensors. In order to enable the FIFO data buffer, the global enable switch `FIFO_CONF.fifo_en` has to be set to 0b1 and at least one of the signal sources Accelerometer or Gyroscope has to be enabled. To disable the FIFO data buffer, it is sufficient to either de-select all sensor data sources or to set the global enable switch to 0b0.

Frame Header Every frame in the FIFO data buffer starts with a 1-byte header. Each bit of this header encodes for a single source, as shown in Table 24. A bit is set if the respective data source is enabled and its data being updated with this particular frame. Sensortime is only reported in the header in case of a dedicated sensortime frame upon buffer overread, see [Buffer Over-reads](#).

Table 24: Format of the 1-byte FIFO frame header

Bit	7	6	5	4	3	2	1	0
Content	0	0	0	Sensortime	0	Temperature	Gyroscope	Accelerometer

Frame Rates The sampling rate of buffer frames in the FIFO buffer is defined by the maximum output data rate of all the sensors enabled for storage in the FIFO buffer. If other enabled sensors have a lower data rate, their previous data will be repeated in the next frames, until new data is available. The availability of new data is indicated by a value of 0b1 of their respective bit in the header, see Table 24. A new frame will only be inserted in the FIFO data buffer if either Accelerometer or Gyroscope are enabled and either of these sources generated a new sample.

Buffer Reads A buffer frame is deleted from the FIFO data buffer after being fully read in a single burst-read access to the register `FIFO_DATA`. When the FIFO data buffer is disabled, reading from `FIFO_DATA` repeatedly returns a value of 0x8000. The handling of partial frame reads is quite important to understand: If a frame is only read partially, it will be repeated completely with the next read from the FIFO data buffer. In case of a buffer overflow between the first partial read and the attempt for the second read, the frame is kept only if `FIFO_CONF.fifo_stop_on_full` is set to 0b1.

Buffer Over-reads When more data is read from the FIFO buffer than valid data is available, an invalid data identifier with a value of 0x8000 is returned for each word read exceeding the valid data.

Optionally, a dedicated sensortime-only frame can be reported before the invalid data identifier is sent by the device. This special frame contains solely the sensor time when the last byte of the last regular frame was read. This function is enabled by setting `FIFO_CONF.fifo_sensor_time` to `DEDICATED_FRAME`. This special frame has the format depicted in Table 25.

Table 25: Format of sensor-time frame

Order	Size [bytes]	Description
0	1	Header indicating sensor-time only (0x10)
1	3	Sensortime, 24 bit

Buffer Overflow In case of an overflow, the FIFO data buffer can either stop recording data or overwrite the oldest data. This behavior is controlled by the register `FIFO_CONF.fifo_stop_on_full`. If `FIFO_CONF.fifo_stop_on_full` is set to 0b0, the FIFO logic will delete the oldest frames to avoid the loss of the newest samples. If `FIFO_CONF.fifo_stop_on_full` is set to 0b1, the newest frame may be discarded when the remaining free space in the FIFO buffer is less than the currently configured size frame to prevent discarding the oldest data. During a read operation from the FIFO buffer by the host, no data at the FIFO buffer tail may be dropped. If the host reads the FIFO buffer at a slower rate than it is filled, it may happen that the sensor needs to drop new data, even if `FIFO_CONF.fifo_stop_on_full` is set to 0b0.

5.7.3 FIFO Buffering Events

The FIFO data buffer supports two kinds of events that can trigger an interrupt on the host:

- FIFO buffer is full, and
- FIFO watermark level above threshold.

The FIFO buffer full event is issued when the FIFO fill level is above the full threshold. The full threshold is reached just before the last two frames are stored in the FIFO data buffer. This event is enabled by setting `INT_MAP_HW.fifo_full_int_map` to a non-zero value.

The FIFO watermark level event is issued when the fill level of the FIFO buffer is equal or above a watermark level threshold defined in the register `FIFO_WATERMARK.fifo_watermark`. In case the threshold is set higher than the buffer size, the interrupt may be triggered more often than expected. This interrupt is enabled by setting `INT_MAP_HW.fifo_wm_int_map` to a non-zero value.

The events occurring during FIFO data buffering are signaled to the host after mapping them with `INT_MAP_HW.fifo_wm_int_map` and/or `INT_MAP_HW.fifo_full_int_map` to the desired interrupt signaling channel, see section 5.9. Reading from the FIFO data buffer automatically clears the corresponding status bits of the mapped interrupt signaling channel, if the fill level drops below the respective threshold. In latched interrupt mode the interrupt pin level also becomes inactive. Manual clearing of the FIFO data buffer's status bits is neither required nor supported. In pulsed mode, an interrupt will be re-triggered after a FIFO buffer read transaction, in case it was not emptied below the configured threshold.

5.7.4 FIFO Buffer Flush

A flush means discarding all data in the FIFO data buffer. It is triggered either directly through the controller or indirectly by a re-configuration of the device. The user can actively trigger a flush of the FIFO buffer by writing 0b1 to `FIFO_CTRL.fifo_flush`. An indirect, automatic flush of the FIFO data buffer is caused by:

- a signal source to be stored in the FIFO data buffer is added or removed, including any change in `FIFO_CONF.fifo_temp_en`,
- a enable or disable of the FIFO enable switch `FIFO_CONF.fifo_en`, and
- a switch between 24 bit and 16 bit representation mode using `LEGACY_CONF.legacy_range_conf`.

Changes of the device configuration, that do not cause a flush of the FIFO data buffer, are:

- any sensor configuration, e.g. power operation mode, range, sample rate (ODR), via `ACC_CONF`, `GYR_CONF`,
- filter configuration through `FILTER_CONF`, and

- FIFO operation mode via `FIFO_CONF.fifo_stop_on_full`.

5.8 Advanced Features

5.8.1 General Configuration

The advanced features of the device can be activated after enabling the feature engine, which is achieved by the following steps:

1. disabling all sensors, except when enabling the feature engine directly after power on or soft reset, then
2. setting `FEAT_ENG_GLOB_CTRL.feat_eng_mode` to 0b11, and then
3. waiting for the feature engine to be initialized by polling `FEATURE_IO_0.feat_eng_state` for the value 0b01.

Note: Advanced features may be incorrectly interpreted if the accelerometer and/or gyroscope are enabled before the feature engine.

The feature engine may be disabled by setting `FEAT_ENG_GLOB_CTRL.feat_eng_mode` to 0b0. Configurations on the extended register map are not retained and reverted to their reset values after subsequent enabling. Configuration, state toggling and the data input/output of the features is possible via

- the register interface through the registers `FEATURE_STATUS_0` to `FEATURE_STATUS_3`, `FEATURE_IO_0` to `FEATURE_IO_2` and the input synchronization register `FEAT_ENG_SYNC` for
 - enabling and disabling of advanced features,
 - selecting non-continuously running features,
 - data and status output of the features,
 - configuration of the operation Mode Change Feature (see section 5.10)
- the command interface via the register `CMD` for triggering the execution of selected non-continuously running features
- the configuration interface for features through the registers `FEATURE_DATA_CTRL`, `FEATURE_DATA_TX`, `FEATURE_DATA_RX` and `FEAT_ENG_STATUS`, see Section 7.2.

Configurations through the registers `FEATURE_IO_1` and `FEATURE_IO_2` must be executed using the following procedure:

- write or modify the configuration to `FEATURE_IO_1` and/or `FEATURE_IO_2`, and subsequently
- synchronize the configuration by writing 0b1 to `FEAT_ENG_SYNC.feature_io_sync`.

5.8.1.1 Supported ODR of Advanced Features

The advanced features can operate at almost any output sample rate of the accelerometer. In the two continuous sampling states all features are supported independent of the configured sample rates of the accelerometer. For the duty-cycled operation states (LP/ULP) of the accelerometer Table 26 provides an overview of supported sample rates per feature.

Acceleration sample rate	Generic Interrupt features	Wrist wear wakeup	Wrist gesture detector	Step counter	Significant motion	Activity Recognizer	Tap detector
200	Yes	Yes	Yes	Yes	Yes	Yes	Yes
100							No
50							
25							
12.5							
6.25							
<6.25	No	No	No	No	No	No	

Table 26: Supported sample rates per feature in the duty-cycled power operation states

The device adjusts the sample rate dependent parameters of the features to the currently configured sample rate. Threshold values are independent of the sample rate and therefore not modified. All user configurations are retained and not modified until soft-reset or power down of the device or the feature engine. Hence there's no need to update

any feature configuration when changing the sample rate (ODR) of the accelerometer. Optionally, the operating sample rate of the advanced features can be limited or increased by configuring [FEATURE_ODR_1](#) and [FEATURE_ODR_2](#). In the duty-cycled operation states, an error is indicated by [FEATURE_IO_0.wrng_acc_odr](#) if, for all enabled features, the respective configured or required minimum sample rate (ODR) is not fulfilled by the configured accelerometer sample rate (ODR).

5.8.2 Generic Interrupt

The generic interrupt is a feature designed to detect a simple movement or inactivity in an application by the device.

5.8.2.1 Theory of Operation

The implementation realized through the generic interrupt can be adapted to support different use cases. The theory of operation of this feature is presented in Figure 11. In general, the feature monitors the change in the acceleration signal with respect to a defined reference value. Then, the absolute value of this monitoring is compared against a configurable threshold value. A user adjustable hysteresis is included in this comparator to reduce the likelihood of rapidly repeating events. When the output of the comparator for the selected combination of axes exceeds the configured thresholds for a configured duration, the event is triggered. The event can be cleared again, when the condition remains false for a configured wait time.

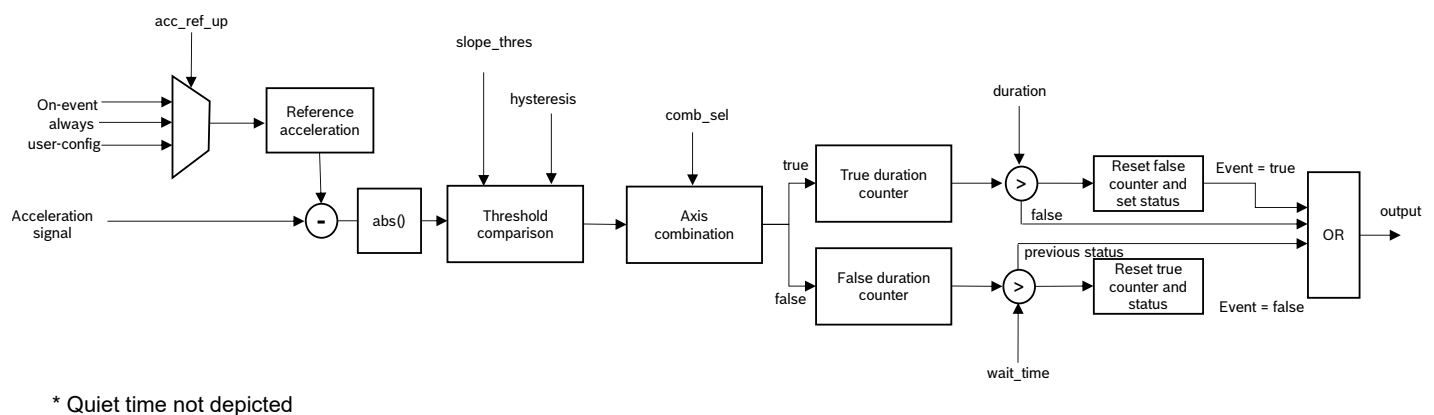


Figure 11: Theory of Operation of the Generic Interrupt

The product contains four pre-configured instances of the generic interrupt feature. These are pre-configured to [Any-motion Detection](#), [No-motion Detection](#), [High-g Detection](#), and [Low-g Detection](#). Their individual behavior will be explained in the following sub-sections.

Each instance has their own individual configuration options for the selection of axis combination, the update of the acceleration reference, the slope threshold and hysteresis, and the timing parameters for attack, release and quiet duration. These have the following influence on the features:

- the selected axis combination defines, which axis or combination of axis is taken for the evaluation,
- the slope threshold influences the detection sensitivity with the sensitivity decreasing for growing thresholds,
- the hysteresis influences the detection sensitivity with lower likelihood for re-triggering the event with higher hysteresis values, that means the hysteresis value determines how much the slope has to increase again after dropping below the threshold to re-trigger the event,
- the attack time defines the duration of the motion being above the given threshold before an event will be triggered,
- the wait time after a detected any-motion event defines the duration in which the motion must stay below the threshold before the event is cleared, and
- the quiet time defines the duration of quietness or “silence” after an event, before a new event can be triggered.

The configuration to include only a single axis in the detection is recommended only if necessary for an application.

The host can enable the features individually as detailed in the following sub-sections. The reporting of the detected events to the host can be mapped to the available event reporting channels of interrupt lines or IBI, see subsection [5.9.1](#). The events can also be used to toggle between main and alternative power operation state, see section [5.10](#). In case any of these generic interrupts is enabled and detected, this is reported combined with all other potentially enabled

events of the generic interrupt instances in the event status register that corresponds to the earlier configured event reporting channel. In case several instances are enabled, the host can determine the source of the detected event through [FEATURE_STATUS_0](#).

5.8.2.2 Any-motion Detection

The any-motion detection feature recognizes changes in the motion by interpreting the slope between adjacent samples of the acceleration signal. It triggers this event, when the slope between adjacent acceleration samples exceeds a threshold for a duration. The feature can be enabled through [FEATURE_IO_2.en_gen_int_anymo](#). The behavior of the any-motion detector can be adapted to the context of the application by configuring the parameters in [GEN_INT_ANYMO_1.axis_sel_anymo](#), [GEN_INT_ANYMO_1.slope_thres_anymo](#), [GEN_INT_ANYMO_2.hysteresis_anymo](#), [GEN_INT_ANYMO_3.duration_anymo](#), [GEN_INT_ANYMO_3.wait_time_anymo](#), and [GEN_INT_ANYMO_4.quiet_time_anymo](#).

5.8.2.3 No-motion Detection

The no-motion detector feature recognizes quasi-static states of the device by interpreting the slope between adjacent samples of the acceleration signal. It triggers this event, when the slope between adjacent acceleration samples remains smaller than a threshold for a defined duration. The feature can be enabled through [FEATURE_IO_2.en_gen_int_nomo](#). The behavior of the no-motion detector can be adapted to the context of the application by configuring the parameters in [GEN_INT_NOMO_1.axis_sel_nomo](#), [GEN_INT_NOMO_1.slope_thres_nomo](#), [GEN_INT_NOMO_2.hysteresis_nomo](#), [GEN_INT_NOMO_3.duration_nomo](#), [GEN_INT_NOMO_3.wait_time_nomo](#), and [GEN_INT_NOMO_4.quiet_time_nomo](#).

5.8.2.4 Low-g Detection

The low-g detection feature is meant to detect low accelerations, sometimes also called free-fall, in applications, e.g. preparation before hitting hard surfaces. This feature can be enabled through [FEATURE_IO_2.en_gen_int_lowg](#). Here, the absolute value of the acceleration vector is monitored. The magnitude of the acceleration vector is compared to the threshold in [GEN_INT_LOWG_1.slope_thres_lowg](#). The event will be generated when the magnitude of the acceleration is smaller than the threshold for the duration configured in [GEN_INT_LOWG_3.duration_lowg](#). The event is deactivated when the delta of the acceleration magnitude is exceeding the hysteresis in [GEN_INT_LOWG_2.hysteresis_lowg](#).

5.8.2.5 High-g Detection

The high-g detection feature is meant to detect large accelerations in applications, e.g. to disable certain components or to react on user input. This feature can be enabled through [FEATURE_IO_2.en_gen_int_highg](#) and the monitored sensing axis selected in [GEN_INT_HIGHG_1.axis_sel_highg](#). The event is asserted if the absolute acceleration value of at least one enabled axis exceeds the threshold programmed in [GEN_INT_HIGHG_1.slope_thres_highg](#) and the sign of the value does not change for at least the duration configured in [GEN_INT_HIGHG_3.duration_highg](#). The event is cleared either when the absolute value of the acceleration vector of all selected axes drops below the threshold in [GEN_INT_HIGHG_1.slope_thres_highg](#) subtracted by the hysteresis in [GEN_INT_HIGHG_2.hysteresis_highg](#), or if the sign of the acceleration value toggles.

If any device axis is parallel to the gravitational force, then that axis has a value corresponding to 1g or -1g. To avoid undesired frequent reporting of events, it is recommended to configure threshold and hysteresis such, that their difference is greater than 1g. In case the difference of threshold and hysteresis is less than 1g, then after a high-g event is triggered, the event will not get cleared if any of the axis is parallel to the gravitational force since that axis will already be at 1g.

The behavior of the high-g detector can be further adapted to the context of the application by configuring the remaining parameters in [GEN_INT_HIGHG_3.wait_time_highg](#) and [GEN_INT_HIGHG_4.quiet_time_highg](#).

5.8.3 Significant Motion Detection

The significant motion detection provides an event raised on detection of a significant motion as defined in the Android⁷ specification⁸.

This feature is supported in the high performance power operation mode for all sample rates and in the low power operation mode for the sample rates from 50 Hz to the maximum supported sample rate. It can be enabled by setting [FEATURE_IO_2.en_sig_motion](#) to 0b1.

In Android, a significant motion is a motion due to a change in the user location or behavior. Examples of such significant motions are walking or biking, sitting in a moving car, coach or train, etc. Examples of situations that typically do not

⁷Android is a trademark of Google LLC.

⁸https://source.android.com/devices/sensors/sensor-types.html#significant_motion

trigger significant motion events include for example “phone in pocket and person is stationary” or “phone is at rest on a table”. Upon detection of a user movement classified as significant according to the aforementioned examples, an event is raised indicating the probable change of a user location. Classification of movement as significant motion or not is based on the analysis of the acceleration signal over a configurable duration of time. This time is adjustable by the segment size in `SIGNIFICANT_MOTION_1.segment_size`. Time segments are assumed to be non-overlapping. If the significant motion condition is evaluated as true for greater than 50% of the configured duration, an event is raised.

Example An example for the behavior of the significant motion detection in a walking scenario is depicted in Fig. 12. Here, the segment size is set to 5 seconds (0x00FA).

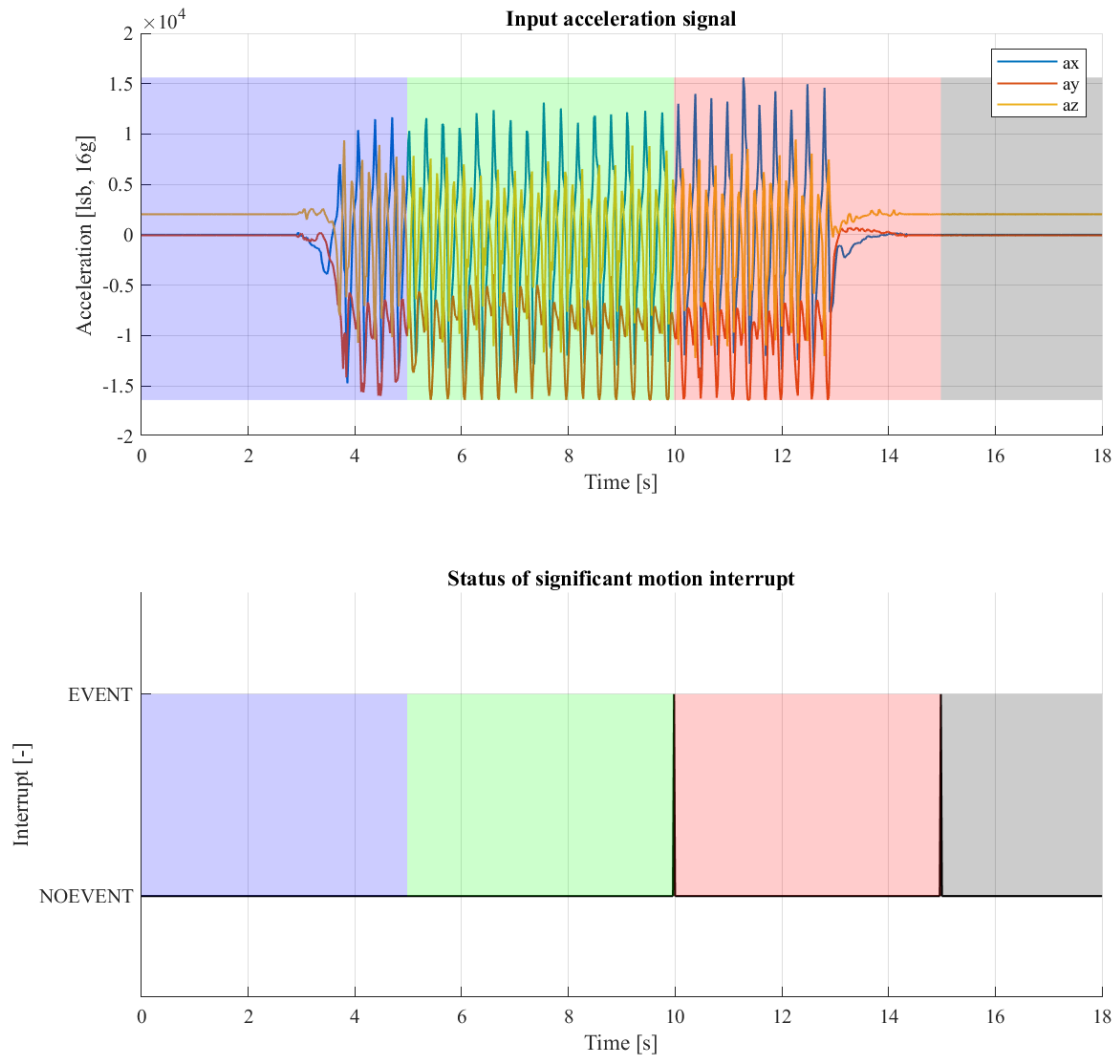


Figure 12: Significant motion detection behavior for walking use-case

This example contains 3 scenarios of motion within the configured segment size and therefore time interval:

1. Large initial part of segment as STILL with small part of segment as WALKING.
2. Full segment as WALKING.
3. Initial large part of segment as WALKING with remaining being STILL.

Segment #1 marked in blue encompasses the user motion for less than 50% of `SIGNIFICANT_MOTION_1.segment_size`, hence no event is asserted here. In contrast to that, segment #2 in green and segment #3 highlighted with red include the user motion for greater than 50% for which the events are reported at the end of the segment.

5.8.4 Step Counter and Step Detection

The Step Counter provides the function required for counting of steps as defined in Android⁹ ¹⁰. The Step Detector implements the function required for step detection in Android¹¹. In this product, the algorithm for counting steps is designed for smartphone use cases and optimized for accuracy, while the algorithm for the detection of steps is optimized for reporting of step detection events with low latency. Each event can be enabled independently. These features are supported in the high performance power operation mode for all sample rates and in the low power operation mode for the sample rates starting from 25 Hz to the maximum supported sample rate.

Step Counter The Step Counter accumulates the steps detected by the step detection event and provides the current value of the step count. The host can receive an event every time a certain number of steps occurred. This event is realized with a watermark level. When the watermark level is exceeded by the actual step count, the corresponding event is asserted for the mapped interrupt channel, see section 5.9. Example: if the watermark level is set to 200, an event will be raised after every interval of 200 steps. As the steps are buffered internally, the output may be triggered between 200 to 210 steps. The value of accumulated steps stored in the internal buffer can be reset on user demand by activating a flag. When activated, the value of this flag is automatically reset and counting is restarted. The accumulated step count value can be reset while any of the features Step Counter or Step Detector is enabled.

The feature is enabled via [FEATURE_IO_2.en_step_count](#). The actual number of steps is reported in [FEATURE_STATUS_2.step_count_15_0](#) and [FEATURE_STATUS_3.step_count_20_16](#). The watermark level configuration and the step count reset flag are accessible via [STEP_COUNTER_1.sc_wm_level](#) and [STEP_COUNTER_1.reset_counter](#). An update in the step count is reported for the configured event reporting channel in the corresponding event status registers as described in section 5.9.

Step Detector The Step Detector triggers an event for every newly detected step on the configured event signaling channel and the corresponding status bit is set. The Step Detector feature is optimized for low latency to allow for a fast reaction by the host in case of such an event. Hence, when a step is detected, it is immediately signaled. Due to this behavior, there may exist situations when the sum of the detected steps is different than the Step Counter value.

The feature is enabled via [FEATURE_IO_2.en_step_detect](#). A detected step is notified to the host through the configured event reporting channel and in the corresponding event status register as described in section 5.9.

5.8.5 Tap Detection

The device allows the detection of different tap gestures. Supported tap gestures include the single-tap, double-tap and triple-tap. The feature is supported in the continuous power operation modes for all sample rates and in the duty-cycled power operation modes for 200 Hz sample rate only, see Table 26

Enable and disable Each gesture can be individually enabled and disabled via following fields:

- [FEATURE_IO_2.en_single_tap](#)
- [FEATURE_IO_2.en_double_tap](#)
- [FEATURE_IO_2.en_triple_tap](#).

Status output When a tap gesture is detected, each kind of gesture is reported individually in the feature status register [FEATURE_STATUS_0](#) as well as 'or'- combined in the interrupt status register, if the interrupt source is mapped. For example, if mapped to INT1, the interrupt status is available in:

- [INT_STATUS_INT1.tap_det_int1](#)
- [FEATURE_STATUS_0.status_single_tap](#)
- [FEATURE_STATUS_0.status_double_tap](#)
- [FEATURE_STATUS_0.status_triple_tap](#)

⁹Android is a trademark of Google LLC.

¹⁰https://source.android.com/devices/sensors/sensor-types.html#step_counter

¹¹https://source.android.com/devices/sensors/sensor-types.html#step_detector

The status of the detected tap gestures is retained until the next gesture detection or until the respective interrupt status field is cleared.

Sensing axis The dominant sensing axis can be configured using [TAP_DETECTOR_1.axis_sel](#). By default, this is selected as the z-axis. Depending on the tap impact and direction, it is also possible to detect tap gestures which are not strictly aligned with the selected axis.

Tap detection principle A tap event is defined as subsequent positive and negative crossing of a threshold within a configured maximum time limit between the crossings. The absolute value of the threshold for a tap detection is programmable via [TAP_DETECTOR_2.tap_peak_thres](#). The maximum time window between the threshold crossings is defined by the parameter [TAP_DETECTOR_3.max_dur_between_peaks](#). To enable tap detection under noisy operating conditions, for a single tap movement, the limit on the number of threshold-crossing can be configured using [TAP_DETECTOR_1.max_peaks_for_tap](#). Further configuration options [TAP_DETECTOR_3.min_quiet_dur_between_taps](#) and [TAP_DETECTOR_3.tap_shock_settling_dur](#) are visualized in Figure 13 and can be used to fine-tune the tap detection.

Classification of a tap gesture The classification of a tap gesture as a double-tap or triple-tap gesture is dependent on the time window in which the 2nd or 3rd tap occurs after the first tap. The time window is set by [TAP_DETECTOR_2.max_gesture_dur](#). For example, in case of a double-tap to be detected, the 2nd tap event has to occur within this limit after the first tap. In case of a triple-tap to be detected, the 2nd and 3rd tap events have to occur within this limit after the first tap.

Reporting behavior of a tap gesture On detection of a tap gesture, the reporting behavior of the event is determined by the value configured in [TAP_DETECTOR_1.wait_for_timeout](#):

- set to 0b0: each detected tap event is reported. E.g., to detect the triple-tap gesture, the 1st, 2nd and 3rd tap events are reported as single-tap, double-tap and triple-tap respectively, if they are enabled.
- set to 0b1: the corresponding tap gesture is reported after the duration of [TAP_DETECTOR_2.max_gesture_dur](#). E.g., to detect the triple-tap gesture, only the 3rd tap event is reported. No event is reported, if the number of detected taps is less or greater than three.

Quiet time Once a tap gesture is reported, the detection of a further gesture is suspended for a quiet time as defined by the parameter [TAP_DETECTOR_3.quiet_time_after_gesture](#).

Detection sensitivity mode The tap detector offers configurable sensitivity for tap event detection via [TAP_DETECTOR_1.mode](#). The detection modes affects the high-pass filter behavior, and enable a simple selection of sensitivity levels for tap detection, while keeping the values of other configuration parameters unchanged. Further details can be found in the memory map at [TAP_DETECTOR_1.mode](#).

Example To illustrate the working principle of the tap detector, following diagrams are provided. Figure 13 shows the behavior of the tap detector with all supported tap gestures enabled and with [TAP_DETECTOR_1.wait_for_timeout](#) set to 0b0. For every detected tap, the corresponding interrupt is reported if the taps occur within [TAP_DETECTOR_2.max_gesture_dur](#) since the first tap.

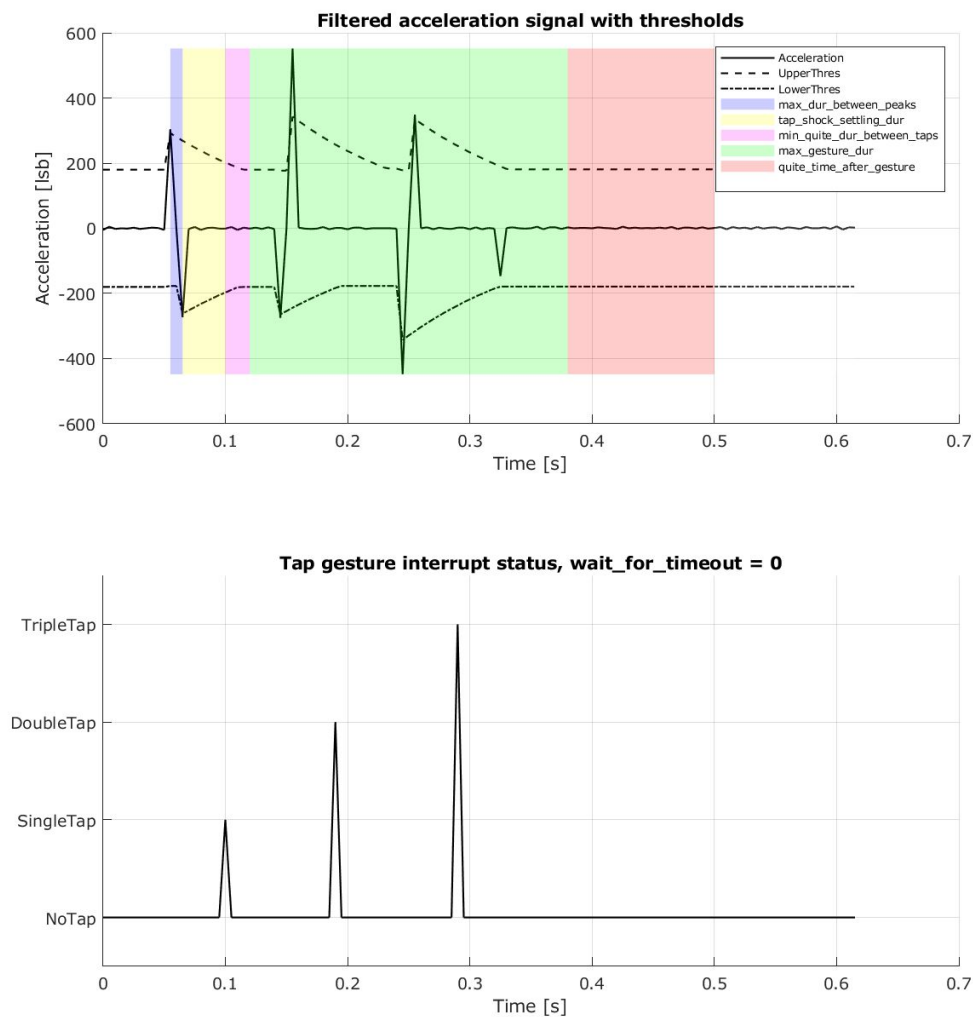


Figure 13: Reporting of tap gesture when `TAP_DETECTOR_1.wait_for_timeout = 0b0`

The tap detector behavior in case of enabling all supported tap gestures and with `TAP_DETECTOR_1.wait_for_timeout` set to 0b1 is depicted in the graphs in Figure 14. As can be seen, only the 3rd tap detected within `TAP_DETECTOR_2.max_gesture_dur` after the first tap is reported.

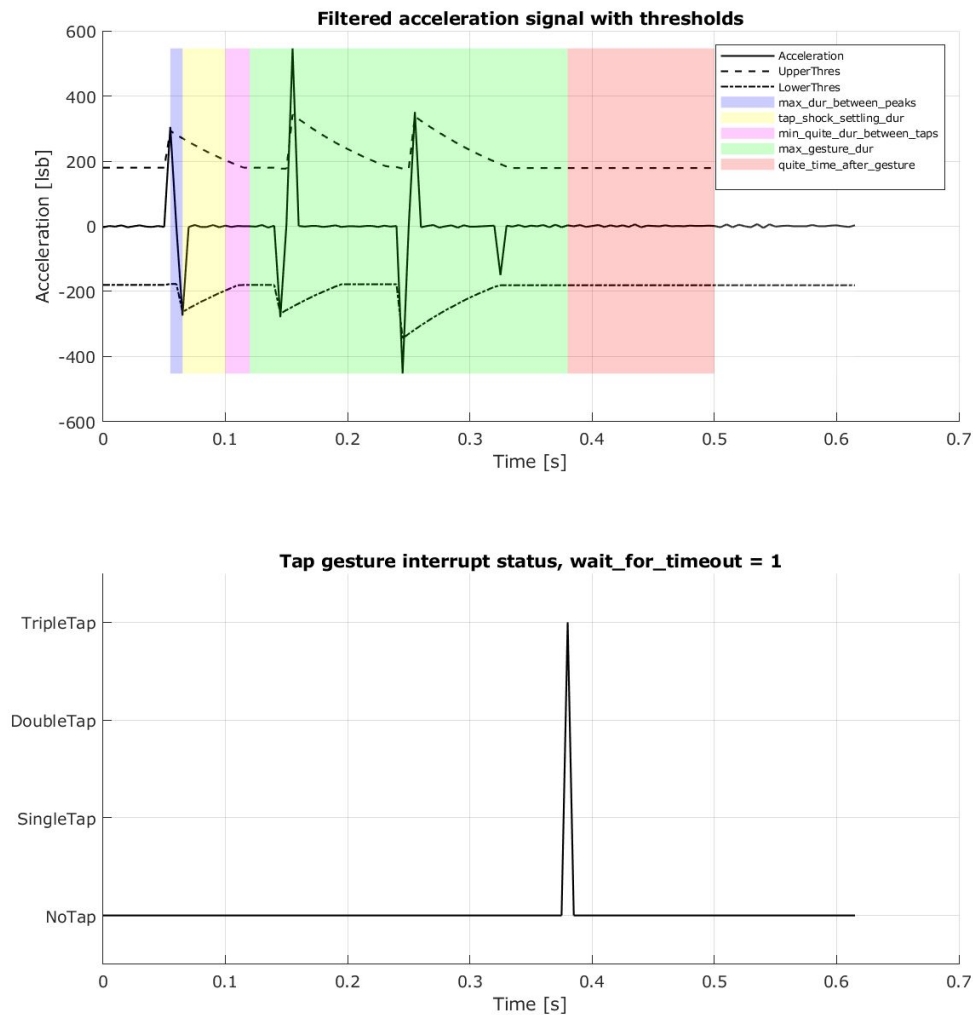


Figure 14: Reporting of tap gesture when `TAP_DETECTOR_1.wait_for_timeout = 0b1`

5.8.6 Wrist Wear Wake-up Detection

The feature to detect a wrist wear wake-up gesture is intended for applications with users wearing a wrist device, e.g. a classical watch. It is intended to be used as gesture detection for any natural movement of the human arm when the user desires to take a look on the wrist device, e.g. the watch face, and expects the screen to be turned on or off depending on the type of gesture. This feature has a dependency on the device orientation in the user system. The interpretation of the movements depends on the device coordinate system. The device/system coordinate frame used in the following for explanation of the function and its configuration is depicted in Figure 15 and assumes that the sensor coordinate frame is aligned with the device/system coordinate frame. For the coordinate system, please also take Subsection 5.11.2 into account.

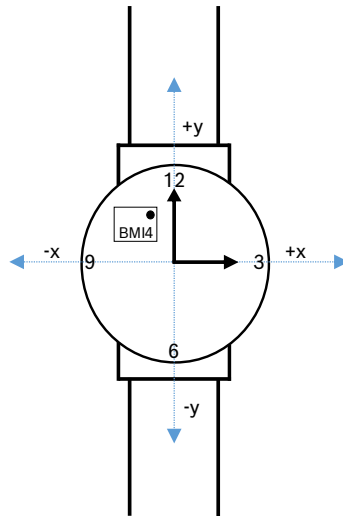


Figure 15: Wrist Wear Wake-Up: Coordinate System

The feature can distinguish if the device is in one of the following two positions:

- Focus position: arm is in front of the body and it is expected, that the user can look comfortably onto the watch face, and
- Non-focus position: the user is not able to look onto the watch face

Two different kinds of gestures are supported and explained in the following: the wake-up event and the drop event.

Wake-up event Two different kinds of movements are supported to be identified as wake event while wearing on wrist:

1. raise the arm to the focus position from a non-focus position, and
2. roll the wrist within the focus position

for the following start and end conditions of a movement:

- device on arm mostly flat, that means horizontal, with watch face looking either upwards or downwards or watch face tilted towards the user, that means portrait up,
- for the case of a device on the left arm, device on arm pointing vertically up, that means landscape left, or pointing vertically down, that means landscape right, and
- relative to the user in-front of the body, sideways to the body or over the body.

To detect an event, the arm position is monitored including the check of additional constraints. First, the arm position is estimated by checking thresholds on the filtered acceleration. This estimated position is then tracked to detect the transition from one position to another. As one additional constraint, the device must be static for arm positions to make sure that continuous (slower) motions of the arm between two consecutive arm positions are not detected as two different positions. This check is conducted by checking if the angle is less than a configurable static state angle threshold for a configurable duration.

To avoid misinterpretation when the wearer of a device is moving, e.g. user motions like walking, climbing stair cases or running, a locomotion detection is incorporated to avoid raising false positives. A detected locomotion limits at the same time the possible arm position transitions. If the locomotion condition is true, detectable gestures are limited to device orientations where the arm is mostly flat or the arm is tilted towards the user while arm positions such as above shoulder level, face down and landscape directions are not supported.

The angle of the arm position is used as further constraint to determine a significant motion of the arm. If the angle is greater than or equal to a threshold for a configurable duration and was static after the last gesture was detected, the condition for a significant motion is true which helps to avoid raising false positive events.

Drop Event The drop detection is intended to observe the reverse transition of the arm once a wake-up event has been detected, that means also leaving the focus position. The detection of a wake event triggers the check for drop until the drop detection is disabled. The drop detection does not interfere with the wake detection because it re-uses the states of

the wake detection to determine a drop event.

One of the following conditions must be fulfilled for detecting a drop event by a change in arm position:

1. Change of the arm position in reverse direction: at the time of a detected wake, the arm position is recorded and compared to the change to a new arm position in which the arm must be retained for a configurable duration. If the change between the positions corresponds to the reverse, a drop event is raised. Note, that if locomotion is detected, the same additional position checks are performed as for the wake event.
2. Change of the arm position during significant motion: the arm position at the start of the significant motion is recorded and compared to the recorded arm position once the significant motion ends. If the interpreted motion does not correspond to a transition satisfying the conditions for a wake, a drop event is raised.

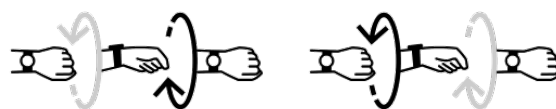
User Interface The feature can be enabled and disabled through [FEATURE_IO_2.en_ww_wakeup](#). The detection of a drop event after detection of a wake event is enabled or disabled with [WRIST_WEAR_WAKEUP_6.enable_drop](#). The feature reports its status through [FEATURE_STATUS_1.status_ww_wakeup_drop](#).

The settings [WRIST_WEAR_WAKEUP_1.angle_portrait_down](#), [WRIST_WEAR_WAKEUP_1.angle_portrait_up](#), [WRIST_WEAR_WAKEUP_2.angle_landscape_left](#), and [WRIST_WEAR_WAKEUP_2.angle_landscape_right](#) allow to configure the sensitivity to reach a focus position. The configurations [WRIST_WEAR_WAKEUP_3.min_angle_non_focus_pose](#) and [WRIST_WEAR_WAKEUP_4.min_angle_focus_pose](#) can be used to adjust the sensitivity of the angle to detect a wake-up as well as drop event and of the detection of a significant motion. The setting [WRIST_WEAR_WAKEUP_5.min_dur_static](#) provides the possibility to adapt the expected minimum duration of the arm in a static state between two consecutive gestures. The minimum duration for detection of a significant motion can be configured via [WRIST_WEAR_WAKEUP_5.min_dur_in_motion](#).

If the configuration [WRIST_WEAR_WAKEUP_6.enable_arm_stretch_pulldown](#) is enabled, the additional arm position of "arm above shoulder" is supported and detected when the arm is raised by 90 degree to the elbow or the arm is raised above the shoulder. This arm position helps to distinguish between the raising of the arm above the body while lying down and the raising of the arm above the shoulder level while sitting or standing.

5.8.7 Wrist Gesture Detection

The device is designed to support Wear OS by Google™ and features the detection of the wrist gestures flick-in, flick-out, and wrist jiggle/shake to enable [quick, one-handed interactions with apps on a smartwatch](#) when a touch screen is inconvenient. The movements of the wrist to trigger such events are explained graphically in the Figs. 16a, 16b and 17. The interpretation of the movements depends on the device coordinate system. The device/system coordinate frame used in the following for explanation of the function and its configuration is the same as for the wrist wake-up gesture provided Figure 15 and assumes that the sensor coordinate frame is aligned with the device/system coordinate frame. For the coordinate system, please also take Subsection 5.11.2 into account.



(a) Flick-in Movement

(b) Flick-out Movement

Figure 16: Wrist Wear Navigation Gestures: Flick in/out

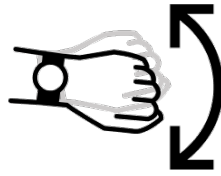


Figure 17: Wrist wear Navigation Gesture: Shake/Jiggle Movement

For detection of a flick-in navigation gesture as shown in Fig 16a, the user must slowly turn the wrist away from the body, that means roll-out as indicated with the light-grey arrow, and then quickly bring it back to the outgoing position, that means roll-in as depicted with the darker-black arrow. This can be used to scroll up the notification list or to scroll up the menu when it is displayed in the app drawer. For the detection of the flick-out gesture explained in Fig. 16b, the user must quickly turn the wrist away from the body, that means roll-out shown with a darker-black arrow, and then slowly return it back to its outgoing position, that means roll-in indicated with the light-grey arrow. Common use-case is to scroll down a list of notifications or scroll down the menu list when opened by the app drawer.

The shake gesture, also known as jiggle gesture, has to be performed by the user by holding the arm in front in a orientation close to horizontal. Then, the wrist must be turned away from and towards the body for few times where the turns need not be made too fast and too long. A typical functionality to be supported is to navigate to the start screen of the wearable device. For Wear OS devices, shaking the wrist is the system-wide back or undo gesture.

Unambiguous interpretation of user movements demands the feature to be configured whether the device is worn by the user on either the left wrist or the right wrist.

The gesture detection has an adjustable de-noising of the acceleration signal to allow customization to applications and users. The gesture detection is initiated by the detection of a focus pose of the face view. The orientation of the focus pose including the detection sensitivity can be configured via a gravitation window in the X axis and independent thresholds for the gravitation on the Y and Z axis, respectively. If there is minimal movement in the Z direction, the gesture is classified as:

- Flick In when an acceleration peak is detected in the +Y direction,
- Flick Out when an acceleration peak is detected in the -Y direction, and
- if the number of acceleration peaks in any Y direction equals or exceeds four regardless of movement in the Z direction, the gesture will be classified as a Jiggle.

The feature can be enabled and disabled through [FEATURE_IO_2.en_wg_detector](#). The status whether and which gesture was detected can be obtained from [FEATURE_STATUS_1.wrist_gesture](#). The wrist wear position is configured in [WRIST_GESTURE_DETECTOR_8.device_wear_position](#). The focus pose for face view detection is configured through [WRIST_GESTURE_DETECTOR_3.gravity_bound_x_neg](#), [WRIST_GESTURE_DETECTOR_4.gravity_bound_x_pos](#), [WRIST_GESTURE_DETECTOR_5.gravity_bound_y_neg](#), and [WRIST_GESTURE_DETECTOR_6.gravity_bound_z_neg](#).

The sensitivity for the detection of a flick-in or flick-out gesture is controlled by [WRIST_GESTURE_DETECTOR_1.min_flick_peak_y_threshold](#) and [WRIST_GESTURE_DETECTOR_2.min_flick_peak_z_threshold](#).

5.8.8 Voice Activity Detection

The device can detect activity of voice by a voice activity detector (VAD). This detector analyzes the acceleration signal of structure borne vibrations sensed through the accelerometer while a user is speaking. The analysis is done by segmentation of the signal in the time domain and followed by a classification as voice or non-voice. In applications such as hearable devices, one can use this VAD to detect with ultra-low power consumption the voice of the user wearing it. It is assumed, that the user is wearing a hearable device attached to a vibration conducting structure such as the human skull. On the one hand, the VAD is designed to recognize whether the user is speaking or not, and on the other hand to reject environmental noise. To optimize power consumption, it is in most cases sufficient to use only one sensor axis. The most relevant axis for voice activity detection can be determined for example through mechanical simulations of the application followed by confirmation through the analysis of recorded data by the sensor in the target application. On detection of voice/speech, the VAD triggers an event and provides in addition status information on the voice. The algorithm supports two different classification modes for VAD:

- **Sensitive:** High detection rate for voice events at the expense of possible false positives (falsely detected voice events). Typically, this configuration has the lowest detection latency.
- **Robust:** Reduce the false positives as much as possible while still having high detection rate of voice events. Typically, this configuration has the highest detection latency.

An event from the VAD can be used as interrupt to enable use cases such as keyword recognition, voice enhancement and other speech processing functionalities.

The VAD feature is activated or deactivated by setting `FEATURE_IO_2.en_vad` to enabled (0b1) or disabled (0b0) when the accelerometer of the device is activated in normal or high performance power state. It is possible to configure one or a combination of axis of the acceleration signal used for analysis and classification as voice through `VAD_1.en_vad_chnl`. The two different classification modes for VAD can be configured via `VAD_1.cls_mode`.

5.8.9 Activity Recognition

Please consult Bosch Sensortec for dedicated application notes detailing configuration and usage of this feature.

5.8.10 Low Power Wake Up

The low power wake-up feature detects changes in the motion by interpreting the slope between adjacent samples of the acceleration signal. It works similarly to the Any-Motion feature described in section 5.8.2.2, however it is operated independent of the feature engine and can be used to wake it up in combination with the automatic mode switch, as described in section 5.10. The low power wake up can be enabled for individual or multiple acceleration axes by `LPWUP_EN.lpwup_x_en` to `LPWUP_EN.lpwup_z_en`. Additionally the detection of the end of the condition on all enabled axis can be turned on via `LPWUP_EN.lpwup_end_en`.

A low power wake up event is detected if any of the enabled axes exceeds a threshold configured for a consecutive number of samples. As soon as all enabled axes fall or remain below this threshold for the same number of samples, the end of the event is detected.

The two configuration options to adjust the detection characteristic for this feature are

- **Threshold**, the limit in *mg*, above or below which the slope of two adjacent acceleration samples have to be to count for the duration. Configurable via `LPWUP_CFG.lpwup_ths`.
- **Duration**, the number of samples, which have to exceed or undercut the threshold before the event or its end is detected. Configurable via `LPWUP_CFG.lpwup_dur`.

The value is converted into a time in seconds by dividing the sample count with the configured sample rate (ODR).

Note: This feature is intended to be used in Low-Power operation modes. Due to higher sampling rates in continuous sampling operation modes, the detection behavior will differ.

Figure 18 shows exemplary the detection of the start and end of a low power wake up event for a single enabled axis.

The detection of an event by the low power wake up feature is indicated in `LPWUP_STATUS`. The field of the triggering axis or `LPWUP_STATUS.lpwup_end`, in case of a detected end, then reads as 0b1. Furthermore, this can also be signaled via any signaling channel using `INT_MAP_HW.lp_wup_int_map` (see section 5.9.1 for further details).

5.9 General Event Signaling Configuration

The signaling of interrupts to the host is possible via the I3C in-band interrupt (IBI) feature and two electrical pins. When using the I3C protocol, the IBI feature as well as the two interrupt pins can be used at the same time to signal interrupts to the host. When the protocols SPI and I²C are used, signaling of interrupts to the host is only possible via the interrupt pins INT1 and INT2.

5.9.1 Interrupt Mapping and Acknowledgment

The mapping of a feature interrupt to a signaling channel can be configured through the registers `INT_MAP_HW` and `INT_MAP_FEAT_ENG`. Each feature is mapped exclusively to one of the three signaling channels using the scheme stated in Table 27.

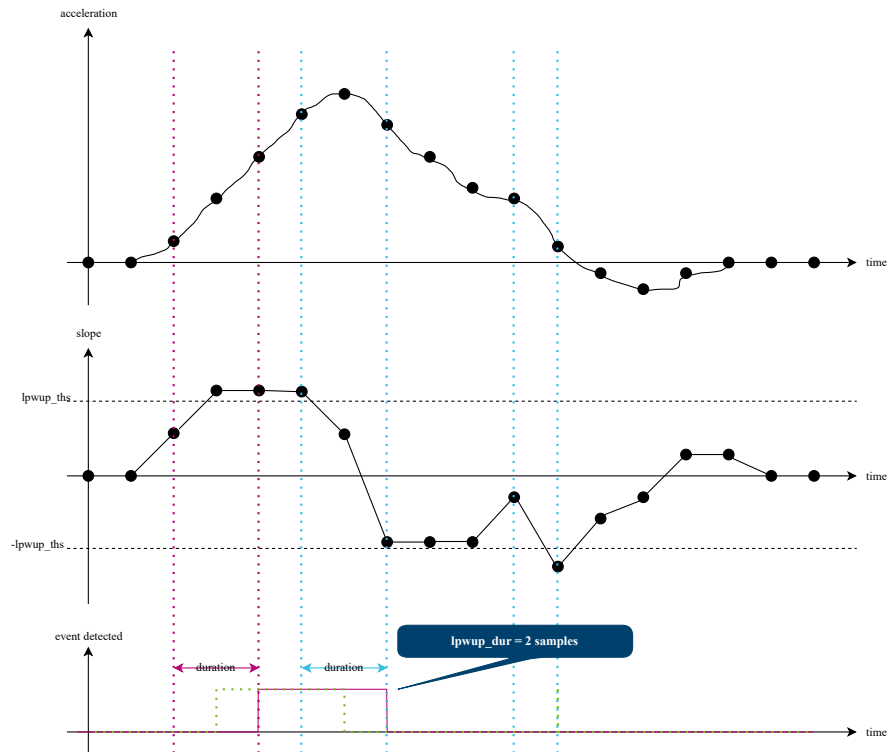


Figure 18: Low Power Wake Up event detection

Table 27: Interrupt mapping to signaling channel

Map mode	Behavior
0b00	Signaling of interrupt disabled
0b01	Signaling of interrupt on INT1 pin
0b10	Signaling of interrupt on INT2 pin
0b11	Signaling of interrupt via I3C IBI

For each interrupt signaling channel, a dedicated interrupt status register is present in the register map of the device:

- the INT1 pin has the corresponding status register [INT_STATUS_INT1](#),
- the INT2 pin has the corresponding status register [INT_STATUS_INT2](#), and
- the in-band interrupt feature of I3C has the corresponding status register [INT_STATUS_IBI](#).

Once an interrupt is notified to the host via a configured signaling channel, its dedicated bit-flag is set in the corresponding status register. In case multiple interrupts are mapped to the same channel, the host can determine the source of an interrupt through the status bits of the corresponding signaling interface.

The bits of a status register can be cleared altogether in a clear-on-read (CoR) fashion by reading the register, which is the default behavior. Alternatively, the status registers can be configured to a clear-on-write (CoW) scheme via [HIF_CONFIG.cor_config](#). With CoW, status registers will preserve their value after being read and can be cleared selectively by writing 0b1 to the corresponding interrupt status bit. Unmapping an interrupt from a signaling channel also clears its bit-flag in the respective status register.

Note: status bits of the FIFO data buffer events have a special behavior as described in section 5.7.3 and do not need to be cleared manually.

5.9.2 Electrical Interrupt Pin Behavior

The electrical behavior of interrupt pins INT1 and INT2 can be configured in the registers [INT_CONF](#) and [IO_INT_CTRL](#). Their electrical output can be enabled via [IO_INT_CTRL.int1_output_en](#) and [IO_INT_CTRL.int2_output_en](#), respectively. This is not applicable to the I3C IBI feature. Both interrupt pins can be configured to have the desired

Table 28: Pulse duration in short and long pulsed mode

	Short pulsed mode	Long pulsed mode
Typ. pulse duration	1.8 μ s	39 μ s

- electrical drive characteristic,
- active level of the interrupt, and
- interrupt output mode.

The characteristic of the output driver of the interrupt pins may be configured with bits `IO_INT_CTRL.int1_od` and `IO_INT_CTRL.int2_od`. By setting these to 0b1, the output drivers show open-drain characteristic, by setting the configuration bits to 0b0, the output drivers show push-pull characteristic.

The electrical output level of the interrupt pins, whenever an interrupt is triggered, can be configured as either “active-high” or “active-low” via `IO_INT_CTRL.int1_lv1` and `IO_INT_CTRL.int2_lv1`, respectively.

The device supports pulsed and latched interrupt output modes for all available interrupt sources. The mode is selected individually for each interrupt pin by `INT_CONF.int1_mode` and `INT_CONF.int2_mode`.

- In the latched mode, the output of an interrupt pin is active while the status bit of any mapped interrupt source is set. It will remain active until all bits of the respective interrupt status register are cleared, as described in subsection 5.9.1. Latched interrupts are designed for systems using level-triggered interrupts.
- In short and long pulsed mode the interrupt output becomes active when the status bit of any mapped interrupt source is being set. Then, after a set time depending on the selected pulsed mode, the interrupt becomes automatically inactive, while the corresponding status bit remains uncleared. Repeatedly triggered interrupt source, e.g. data ready interrupts cause repeated pulses, independent of their status bit. Table 28 provides the typical pulse duration for short and long pulsed mode. Pulsed interrupts are designed for systems using edge triggered interrupts

Note: If the output mode is set to off, the corresponding interrupt status register will not be updated and cleared.

5.9.3 Interrupt Pin Behavior Example

For a better understanding of the interrupt pin behavior of the device, the following examples under various configurations are provided. For simplicity, “INT pin” represents both INT1 and INT2 pins, and the electrical behavior of the interrupt pins is configured as “active-high”.

Latched Mode Figure 19 shows the timing diagram in latched mode. FEATURE_A represents any non-FIFO buffer interrupt source while FEATURE_B represents either a FIFO_WM or a FIFO_FULL interrupt source. Both are mapped to a common INT pin. Detailed explanations of the timing diagram are provided below:

- When the interrupt event “1” of FEATURE_A is triggered, the corresponding FEATURE_A_int_status is set immediately to high. FEATURE_A_int_status is cleared again after the host executes the clear operation at “2”.
- When the interrupt event “3” of FEATURE_B is triggered, the corresponding FEATURE_B_int_status is set immediately to high. The interrupt event “3” of FEATURE_B remains active as long as the FIFO interrupt condition holds true. FEATURE_B_int_status is cleared automatically at “4” after emptying the FIFO below the threshold of the respective FIFO interrupt.
- The INT pin is set to high as long as at least one interrupt status is active.

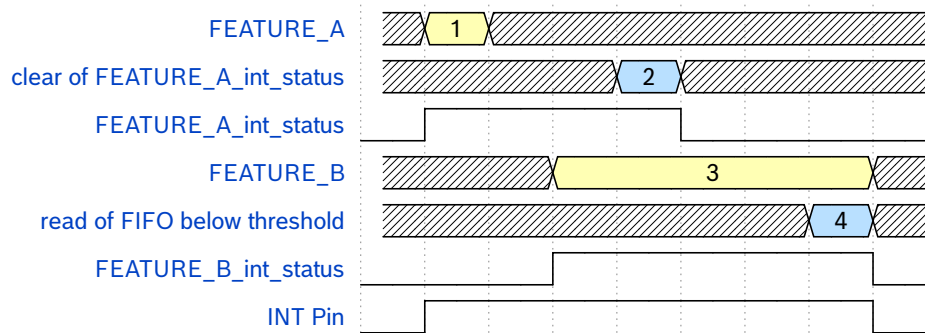


Figure 19: Interrupt output in latched mode

Pulsed Mode Figure 20 shows an interrupt example in pulsed mode. FEATURE_A represents any non-FIFO buffer interrupt source and FEATURE_B represents either FIFO_WM or FIFO_FULL interrupt source. Both are mapped to a common INT pin. Detailed explanations of the timing diagram are provided below:

- When interrupt event “1” of FEATURE_A is triggered, the corresponding FEATURE_A_int_status is set immediately to high, analogous to the INT pin. Since pulsed mode is configured, the INT pin becomes inactive after the selected pulse duration, as defined in Table 28. When another interrupt event “2” of FEATURE_A is triggered, another pulse is generated on the INT pin without the FEATURE_A_int_status to be cleared. At the end, FEATURE_A_int_status is cleared after the host executes the clear operation at “3”.
- When interrupt event “4” of FEATURE_B is triggered, the corresponding FEATURE_B_int_status is set immediately to high, along with the INT pin. Since pulsed mode is configured, the INT pin becomes inactive after the selected pulse duration, as defined in Table 28. FEATURE_B_int_status is cleared automatically at “5” after emptying the FIFO below the threshold of the respective FIFO interrupt.

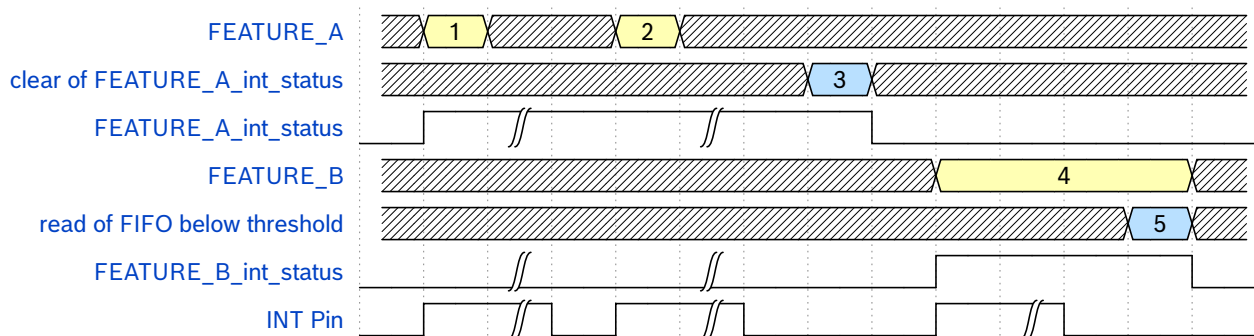


Figure 20: Interrupt output in pulsed mode

5.10 Auto-Operation Mode Change

The auto-operation mode change is a built-in feature to support low-power applications by a smart power management of the device. The feature provides automatic switching among two configuration sets for its accelerometer and gyroscope. The switching is initiated by events of enabled advanced features or by commands sent from the host. In the following, the one set of configurations consisting of `FILTER_CONF`, `ACC_CONF` and `GYR_CONF` for the accelerometer and gyroscope is called user configuration. The other set of configurations consists of `ALT_FILTER_CONF`, `ALT_ACC_CONF` and `ALT_GYR_CONF`, and is called alternative configuration.

Switching between the user and alternative configuration is enabled through `ALT_CONF.alt_acc_en` and `ALT_CONF.alt_gyr_en` for the accelerometer and gyroscope, respectively, and by setting the desired condition for the transitions. The conditions are provided by the feature engine with the advanced features described in section 5.8 and can be configured independently

- through `FEATURE_IO_1.cond_usr2alt_switch` for the switch from the user configuration to the alternative configuration,

and

- through `FEATURE_IO_1.cond_alt2usr_switch` for the switch from the alternative configuration to the user configuration.

By configuring both conditions, a fully automated mode change forth and back can be achieved. Please ensure in that case, that not the same condition is selected for both transition directions. The currently active configuration of both, accelerometer and gyroscope can be read from `ALT_STATUS.alt_acc_active` and `ALT_STATUS.alt_gyr_active` respectively. If `ALT_CONF.alt_rst_conf_write_en` is set to 0b1, either of the sensors can be instantly switched back to the user configuration by writing from the host to either `ACC_CONF` or `GYR_CONF`, respectively.

The auto-operation mode change is complemented by the low power wake-up, see also section 5.8.10. This feature is designed to operate independent of the feature engine. Therefore, it can serve as a mode change condition that triggers even if the feature engine is disabled.

This can be particularly useful in a low power operation state, where no FIFO or any advanced features besides a mode change are required and lowest possible supply current is key. In such a case, the low power wake up can switch the device's sensors into a freely configurable state, e.g. switching from low power to high performance or from accelerometer-only into accelerometer and gyroscope combo mode.

To make use of this, the feature engine and the FIFO have to be either powered down manually via `FEAT_ENG_GLOB_CTRL.feat_eng_mode` and `FIFO_CONF.fifo_en` or automatically by setting `FEATURE_IO_1.dis_feat_eng_fifo_on_switch` to 0b1. The automatic power down occurs when switching to the mode that has low power wake-up set as exit condition.

For a mode change based on the low power wake-up condition, while the feature engine is disabled, the host has to set `FEAT_ENG_GLOB_CTRL.wake_on_trig` to 0b1. Upon a mode switch, the feature engine will then restart the enabled advanced features and, if automatically disabled, restore the previous FIFO configuration.

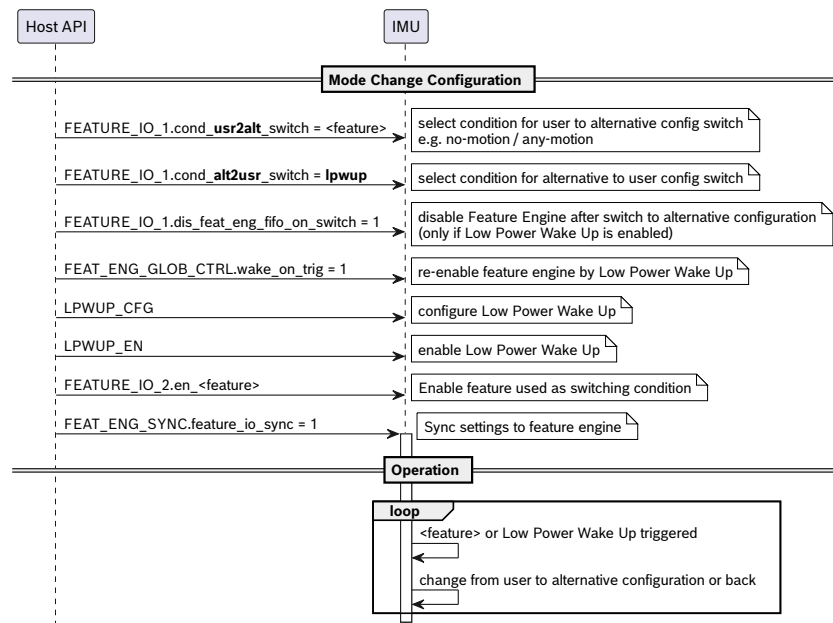


Figure 21: Configuration example of mode change based on Low Power Wake Up

Note: Disabling the feature engine causes a reset of all configuration settings made via the extended register map.

5.11 Application Features

5.11.1 Offset and Sensitivity Error Compensation

The BMI423 supports compensation of sensitivity and offset errors within the accelerometer and gyroscope datapath respectively. Errors as such may be observed in the field or end of line, e.g. due to soldering. In addition the device supports the estimation of the current offset error for accelerometer and gyroscope using integrated algorithms, as

described in sub-section 5.11.1.1.

The respective compensation is automatically performed by the device and applied to any data output, i.e. data registers, FIFO data buffer, if a non-zero value is entered into the following registers

- for the accelerometer
 - offset compensation in 8g range: [ACC_OFFSETS_8G_X](#), [ACC_OFFSETS_8G_Y](#) and [ACC_OFFSETS_8G_Z](#) (applies to 2g and 4g range in 16bit representation, see 5.6.3)
 - offset compensation in 32g range: [ACC_OFFSETS_32G_X](#), [ACC_OFFSETS_32G_Y](#) and [ACC_OFFSETS_32G_Z](#) (applies to 16g range in 16bit representation, see 5.6.3)
 - sensitivity error compensation: [ACC_GAIN_X](#), [ACC_GAIN_Y](#), and [ACC_GAIN_Z](#)
- for the gyroscope
 - offset compensation¹²: [GYR_OFFSETS_X](#), [GYR_OFFSETS_Y](#), and [GYR_OFFSETS_Z](#)
 - sensitivity error compensation: [GYR_GAIN_X](#), [GYR_GAIN_Y](#), and [GYR_GAIN_Z](#)

It is strongly recommended to update these registers only when the affected sensor, either the accelerometer, the gyroscope or both, are disabled to avoid settling of the respective signal after the values are updated. An exception to this are the gyroscope offset compensation registers as described in footnote¹².

To obtain an error compensated output signal s_{cal} , where s is either the acceleration a or the angular rate w , the offset and sensitivity error have to be estimated according to the model

$$s_{cal,\{x;y;z\}} = g_{\{x;y;z\}} \cdot s_{uncal,\{x;y;z\}} + o_{\{x;y;z\}}, \quad (5.2)$$

where $o = (o_x, o_y, o_z)$ and $g = (g_x, g_y, g_z)$ are the offset error and sensitivity error of the uncalibrated signal s_{uncal} . The estimation can either be solely performed by the host and the result entered into the compensation registers or, alternatively, for the accelerometer and gyroscope offset, the host can trigger the device to estimate the error as further described in the following sub-section.

Note: The values contained in the compensation registers can be backed-up in NVM and restored upon power up. For further details see section 5.11.6

5.11.1.1 Automatic Offset Error Estimation

The device supports the automatic estimation of the offset error for the accelerometer and the gyroscope. It is performed individually for each of the two sensors and before the execution, the following preconditions need to be met:

- the respective sensor must be set to a valid configuration in the preferred continuous sampling mode, either normal or high performance mode,
- the alternative sensor configuration must be disabled by setting either [ALT_CONF.alt_acc_en](#) or [ALT_CONF.alt_gyr_en](#) to 0b0,
- the feature engine has to be turned on via [FEAT_ENG_GLOB_CTRL.feat_eng_mode](#), and
- the device is placed at rest, and, in case of the accelerometer, with a configurable axis aligned in parallel to the gravitational axis, via [ACC_OFFSETS_EST_1.axis_1g](#).

The offset error estimation is initiated by writing the respective command into [FEATURE_IO_1.cmd_feature_select](#) as shown in Fig. 22. Once an offset error estimation is running, the data output to the device registers and the FIFO data buffer is disabled, as well as all device features.

While the offset error estimation is in progress, the host is not allowed to modify the configuration of the device to avoid ambiguous results. The device reports the completion of the estimation by setting the register field [FEATURE_IO_0.cmd_handler](#) to 0b0. For precise timing the command execution interrupt ([INT_MAP_FEAT_ENG.cmd_exe_map](#)) can be observed.

After the estimation is completed, the resulting offset error values can be read

- for the accelerometer in 8g range or less from [ACC_OFFSETS_EST_8G_X](#), [ACC_OFFSETS_EST_8G_Y](#) and [ACC_OFFSETS_EST_8G_Z](#).
- for the accelerometer in greater than 8g range from [ACC_OFFSETS_EST_32G_X](#), [ACC_OFFSETS_EST_32G_Y](#) and [ACC_OFFSETS_EST_32G_Z](#).
- for the gyroscope from [GYR_OFFSETS_EST_X](#), [GYR_OFFSETS_EST_Y](#) and [GYR_OFFSETS_EST_Z](#).

¹²Reading or writing the registers [GYR_OFFSETS_X](#), [GYR_OFFSETS_Y](#) and [GYR_OFFSETS_Z](#) requires the gyroscope to be enabled, for example in drive-only power operation state. Signal output has to be discarded during the settling caused by changing these registers.

Additionally, the device can transfer the result directly into the corresponding offset error compensation registers by setting [ACC_OFFS_EST_1.apply_corr](#) or [GYR_OFFS_EST_1.apply_corr](#) to 0b1, respectively.

The behavior of the offset error estimation can be further adjusted via the extended register map in register [ACC_OFFS_EST_1](#) for the accelerometer and in the registers [GYR_OFFS_EST_1](#) and [GYR_OFFS_EST_2](#) for the gyroscope. The configuration options are:

- Gravitational axis: selection of axis aligned in parallel to gravitational axis and its polarity for accelerometer offset error estimation (defaults to positive Z-Axis), via [ACC_OFFS_EST_1.axis_1g](#)
- Number of samples to consider: stabilizing the result in noisy environments, but taking longer time, via [ACC_OFFS_EST_1.samples_to_measure](#) and [GYR_OFFS_EST_1.samples_to_measure](#)
- Signal integrity check: abort offset error estimation if signal standard deviation exceeds a configurable threshold or is zero, via [ACC_OFFS_EST_1.en_sig_int_valid](#) and [GYR_OFFS_EST_1.en_sig_int_valid](#)
- Signal integrity threshold: maximum value for the the standard deviation of the signal, via [ACC_OFFS_EST_1.sig_int_thres](#) and [GYR_OFFS_EST_1.sig_int_thres](#)
- Motion detection: abort gyroscope offset error estimation with [FEATURE_IO_0.cmd_response](#)=ERROR_MOTION_DETECT if accelerometer signal exceeds configurable threshold (requires accelerometer to be in a continuous sampling mode), via [GYR_OFFS_EST_2.en_motion_detect](#)
- Motion detection threshold: maximum value between two acceleration samples, via [GYR_OFFS_EST_2.motion_detect_thres](#)

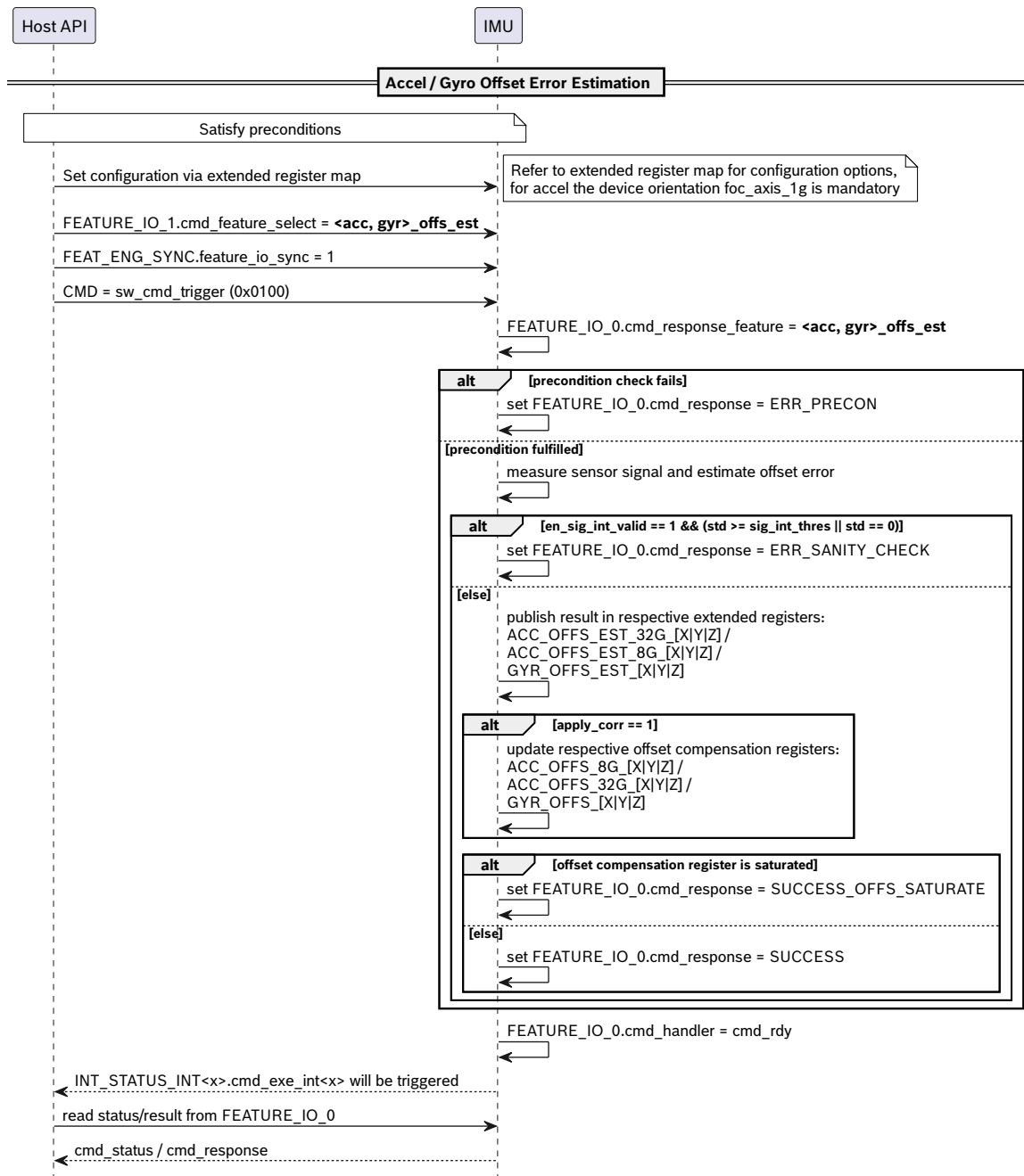


Figure 22: Accelerometer and Gyroscope offset error estimation

5.11.2 Axes Re-mapping and Sign Inversion

The device supports the re-mapping and sign inversion of the sensing axes within the data path. This feature ensures consistent usage of the acceleration and angular rate signals in the algorithms on the device as well as in the processing on the host. It maps the axes of accelerometer and gyroscope to the device orientation as shown in Table 29. The procedure to perform the axis re-mapping and sign inversion is detailed in Fig. 23.

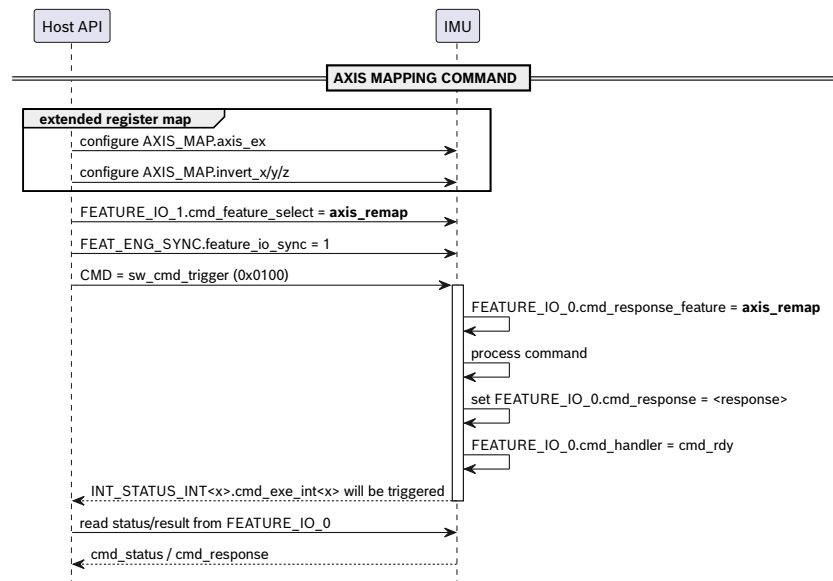


Figure 23: Axes Re-mapping and Sign Inversion Sequence

Axes re-mapping and sign inversion must only be performed when the device is not acquiring data nor computing any advanced feature, for example after power up or after a soft reset. The configuration of the device must not be changed until the completion of the axes re-mapping and sign inversion is signaled.

The desired axes configuration can be selected from Table 29. The corresponding mapping value has to be written to `AXIS_MAP.axis_ex`. The sign inversion of the axis can be interpreted as an axis flip by 180° and is indicated as dashed lines in the figures of Table 29. The inversion setting for x, y and z axis is always according to the selected axes re-mapping configuration. It can be configured individually for each axis according to Table 30 via registers `AXIS_MAP.invert_x`, `AXIS_MAP.invert_y` and `AXIS_MAP.invert_z`, respectively.

The success or failure of the axes re-mapping and sign inversion can be determined by

- monitoring the command execution event via an interrupt pin or I3C IBI, see section 5.9, and
- polling the register `FEATURE_IO_0` and checking the values in the fields `FEATURE_IO_0.cmd_response_feature` and `FEATURE_IO_0.cmd_response`.

Note, that any offset and gain correction values set in registers `GYR_GAIN_X` through `ACC_OFFSETS_8G_Z` will be updated automatically according to new re-mapping and sign inversion to ensure matching to the correct physical sensing axes.

The axes re-mapping and inversion configuration as well as the correction values can be stored in non-volatile memory. During device boot, the latest re-mapping configuration and correction values stored to the non-volatile memory will be applied automatically. If the re-mapping configuration has been changed, the data in non-volatile memory can be updated following the procedure as described in section 5.11.6. Alternatively, the host may save the correction values after re-mapping and restore them after executing the axes re-mapping again after power-up. If axis-remapping and signal correction is performed only once, it's recommended to perform axes re-mapping first.

Table 29: Axes Mapping for Accelerometer and Gyroscope

Value of <code>AXIS_MAP.axis_ex</code>	Mapping ¹³	Figure	Value of <code>AXIS_MAP.axis_ex</code>	Mapping ¹³	Figure
b000	XYZ		b001	YXZ	
b010	XZY		b011	ZXY	
b100	YZX		b101	ZYX	
b110	reserved		b111	reserved	

Table 30: Axes Inversion for Accelerometer and Gyroscope

Value of <code>AXIS_MAP.invert_x/y/z</code>	Description
b0	no inversion (solid line in figures of table 29)
b1	invert (dashed line in figures of table 29)

5.11.3 Self Test

The self-test of the device can be used to check for the correct function of the accelerometer as well as the gyroscope. The execution of the self-test expects the following preconditions to be fulfilled:

- the respective sensor to be tested must be set to a valid configuration in high performance mode, the accelerometer additionally into 8g range

¹³Defines the sequence of the original axis in the new xyz output.

- the alternative sensor configurations for accelerometer and gyroscope must be disabled by setting `ALT_CONF.alt_acc_en` and `ALT_CONF.alt_gyr_en` to 0b0, respectively
- the feature engine has to be turned on via `FEAT_ENG_GLOB_CTRL.feat_eng_mode`, and
- the device is at rest.

The self-test for the accelerometer and the gyroscope is initiated as shown in Fig. 24. It has to be performed for accelerometer and gyroscope individually by writing the respective command into `FEATURE_IO_1.cmd_feature_select`. Once a self test is running, the data output to the device registers and the FIFO data buffer is disabled as well as all device features. Depending on the configuration, the self test takes 60 ms for the accelerometer and 275 ms for the gyroscope¹⁴.

While the self-test is in progress, the host is not allowed to modify the configuration of the device to avoid ambiguous results. The device reports the completion of the self-test by setting the register field `FEATURE_IO_0.cmd_handler` to 0b0. For precise timing the command execution interrupt (`INT_MAP_FEAT_ENG.cmd_exe_map`) can be observed. The result of the self-test can be determined by evaluating the register field `FEATURE_IO_0.cmd_response`. In case the self-test failed, detailed information about the axis causing the failure can be obtained from `ST_RESULT`. After a completed self test, a soft reset or power cycle of the device is not required.

Further configuration options are provided via the extended register map in register `ACC_ST` for the accelerometer and in the registers `GYR_ST_CONF_1` and `GYR_ST_CONF_2` for the gyroscope. The configuration options are:

- Number of samples to consider: stabilizing the result in noisy environments, but taking longer time via `ACC_ST.samples_to_meas` and `GYR_ST_CONF_1.samples_to_measure`
- Number of samples to settle: extending stabilization time before self-test execution via `ACC_ST.samples_to_settle` and `GYR_ST_CONF_1.samples_to_settle`
- Signal integrity check: abort self-test if signal standard deviation exceeds a configurable threshold or is zero, via `ACC_ST.en_sig_int_valid` and `GYR_ST_CONF_1.en_sig_int_valid`
- Signal integrity threshold: maximum value for the the standard deviation of the signal, via `ACC_ST.sig_int_thres` and `GYR_ST_CONF_1.sig_int_thres`
- Motion detection: abort gyroscope self-test if accelerometer signal exceeds threshold (requires accelerometer to be in a continuous sampling mode), via `GYR_ST_CONF_2.en_motion_detect`
- Motion detection threshold: maximum value between two acceleration samples, via `GYR_ST_CONF_2.motion_detect_thres`

¹⁴To achieve the gyroscope self-test timings, the following settings need to be set before the execution: `GYR_ST_CONF_1.samples_to_measure` = 0, `GYR_ST_CONF_1.samples_to_settle` = 3.

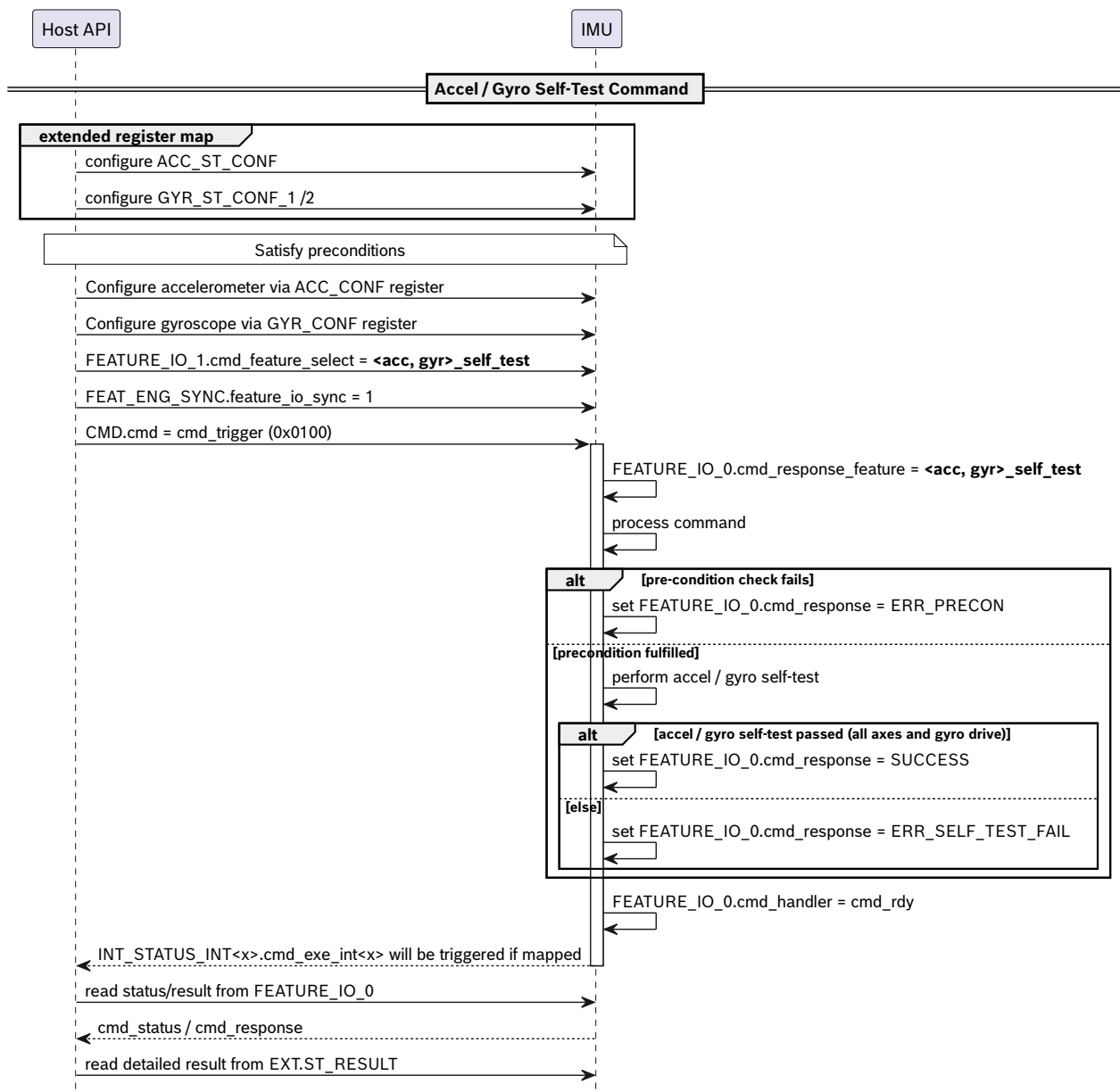


Figure 24: Accelerometer and Gyroscope Self-Test Sequence

5.11.4 Device Health Status

The device reports the status of its health through

- the register [ERR_REG](#) for hardware errors (also accessible via [LEG_ERR_REG](#)):
 - Start-up errors of the device can be retrieved from [ERR_REG.fatal_err](#).
 - Start-up errors of the gyroscope can be retrieved from [ERR_REG.gyr_conf_err](#).
 - Illegal configurations in the registers [ACC_CONF](#) and [GYR_CONF](#) will result in an error code in the fields [ERR_REG.acc_conf_err](#) and [ERR_REG.gyr_conf_err](#), respectively. In this case, the content of the corresponding data registers is undefined. For details, please refer to section 5.6.
 - I3C errors are reported from [ERR_REG.i3c_te0_err](#) to [ERR_REG.i3c_te5_err](#). For details, please refer to section 6.2.3.
- the register [STATUS](#) for data availability information: for details, please check section 5.6.

- the register [FEATURE_IO_0](#) for advanced feature information.
- the register [FEATURE_STATUS_1](#) for the status of the configuration interface for the advanced features.
- the register [FEAT_ENG_STATUS](#) for hardware errors of the feature engine.

With 16 bit data representation enabled, the status for hardware errors and data availability is provided instead through the registers [LEG_ERR_REG](#) and [LEG_STATUS](#).

Reserved bits in these registers are for Bosch Sensortec internal purposes only and can be ignored safely.

5.11.5 Soft Reset

A soft reset can be initiated at any time in all power operation states other than Deep-Suspend by writing the value 0xDEAF for the command “soft-reset” to the register [CMD](#). The soft-reset performs a fundamental reset to the device which is largely equivalent to a power cycle. Following a delay, all user configuration settings are overwritten with their default state wherever applicable. To access the serial interface with any of the protocols SPI, I3C or I2C after a soft reset, the same timing constraints apply as for power on, see chapter 2 for details.

5.11.6 Persistent User Configuration

The device supports persistent user configuration with a few times programmable non-volatile memory (NVM) available on-chip. This memory retains a backup of all registers listed in Table 31 that is automatically restored after soft-reset or power-cycling.

The procedure to update the backup of these registers in NVM needs to be manually triggered by the user from the host and consists of the following steps:

1. Ensure all sensors are in OFF power operation state
2. Value of 0xC0DE has to be written into [CMD](#)
3. Wait for NVM programming time of 130 ms
4. Check field [ERR_REG.nvm_prog_err](#) for a value of 0b0 to detect a successful completion of the operation.

Writing to the NVM always renews the entire NVM contents. Please consider that updating the NVM must not be performed too often as the number of write cycles to the NVM is limited, see also Section 2. It is possible to check the completion of the write process by reading [STATUS.cmd_rdy](#). While [STATUS.cmd_rdy](#) = 0b0, the write process is still in progress; when [STATUS.cmd_rdy](#) = 0b1, writing is completed.

Note: No register write operations should be performed during the NVM write process.

Table 31: NVM-backed registers

GYR_GAIN_X
GYR_GAIN_Y
GYR_GAIN_Z
GYR_OFFSETS_X¹⁵
GYR_OFFSETS_Y¹⁵
GYR_OFFSETS_Z¹⁵
ACC_OFFSETS_32G_X
ACC_OFFSETS_32G_Y
ACC_OFFSETS_32G_Z
ACC_OFFSETS_8G_X
ACC_OFFSETS_8G_Y
ACC_OFFSETS_8G_Z
AXIS_MAP
IO_PAD_STRENGTH

¹⁵Reading or writing the registers [GYR_OFFSETS_X](#), [GYR_OFFSETS_Y](#) and [GYR_OFFSETS_Z](#) requires the gyroscope to be switched to a power operation state other than 'OFF'.

6 Digital Interfaces

The device provides one electrical interface to the host. It acts as a target to the host. This electrical interface is configurable to the serial interface protocols SPI, I²C, and I³C.

6.1 Electrical Specification

The interface is used for device configuration and sensor data readout via digital serial protocols. By default, the device operates in I²C/I³C mode. The interface of the device can be configured to operate in a SPI 4-wire configuration as well. It can also be re-configured to work in 3-wire mode instead of 4-wire mode. All four possible protocols share partly the same pins. The mapping of the interface to the device pins is given in Table 32. The full pin mapping can be found in Table 59.

Table 32: Pin mapping of the digital interface

Pin #	Name	I/O Type	Description	in SPI4W	in SPI3W	in I ² C/I ³ C
1	SDO	Digital I/O	SDO Serial data output in SPI 4W	SDO/MISO	DNC	GND for default I ² C address. VDDIO for alternative I ² C address.
			I ² C / I ³ C Address bit-0 in (selection during boot ¹)			
12	CSB	Digital in	Chip select for SPI mode	CSB	CSB	VDDIO
13	SCx	Digital in	SCK for SPI serial clock ; SCL for I ² C/ I ³ C serial clock	SCK	SCK	SCL
14	SDx	Digital I/O	SDA serial data I/O in I ² C/I ³ C; SDI serial data input in SPI 4W; SDX serial data I/O in SPI 3W	SDI/MOSI	SDX	SDA

In Table 33, the electrical specifications of the interface pins are given.

Table 33: Electrical specification of the digital interface

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pull-up Resistance, CSB pin	R_{up}	Internal Pull-up Resistance to VDDIO	75	100	140	$k\Omega$
Input Capacitance	C_{in}				5	pF
I ² C Bus Load Capacitance (max. drive capability)	$C_{load,I2C}$				400	pF
I ³ C Bus Load Capacitance (max. drive capability)	$C_{load,I3C}$			10	50	pF

6.2 Digital Interface

6.2.1 Protocol Selection

Initially the protocol is automatically selected based on the behavior of the signal on the chip select pin CSB after power-up. After soft reset or power-up, the primary interface of the device is in I²C mode. If the CSB is connected to VDDIO during power-up and not changed, the primary interface works in I²C or I³C mode. The possible switches among the modes on the digital interface are summarized in Table 34.

To use I²C and I³C, it is recommended to hard-wire the CSB line to VDDIO. Since power-on-reset is only executed when both VDD and VDDIO are stable, there is no risk of an incorrect protocol detection due to the power-up sequence. If a rising edge is detected on CSB after power-up, the device interface switches after 200 μs to SPI until a soft reset or

¹More details on I²C / I³C address selection in Subsection 6.2.4.

until the next power-up occurs. Therefore, a rising edge on CSB is needed before starting the SPI communication. It is recommended to perform a single read from a register, e.g. from [CHIP_ID](#), before the actual data exchange with the device. Note: the content of the retrieved data will be invalid.

After the device has been set to the selected protocol once, automatic protocol selection based on CSB can be disabled and the current selection can be made persistent by manipulating [IO_PAD_STRENGTH.if_proto_force](#). The content of this register can be saved to the on-device memory to restore the after each power-up or soft-reset as described in section [5.11.6](#).

The switch from I²C to I³C follows the I³C specification. Upon power up, the chip stays in I²C mode and once the dedicated Broadcast I³C Address (7'h7E) is seen on the bus, the chip will disable its I²C feature and the interface stays in the I³C mode until a soft reset or the next power-up occurs.

Table 34: Protocol Selection for the Digital interface

protocol switch	to I ² C	to I ³ C	to SPI
from I ² C	n/a	Device ID 7E sent	dummy SPI read
from I ³ C	power-down or soft-reset	n/a	dummy SPI read
from SPI	power-down or soft-reset	power-down or soft-reset	n/a

6.2.2 SPI Protocol

The SPI interface of the device encompasses two orthogonal aspects, namely 3-wire or 4-wire interface and mode 0 or mode 3 configuration. The signaling conventions applicable to the supported SPI modes are defined in Table [35](#).

Table 35: SPI mode 0 and mode 3 configuration

SPI mode	Description
0	CPOL = 0 and CPHA = 0
3	CPOL = 1 and CPHA = 1

The automatic selection between mode 0 ('00') and mode 3 ('11') is controlled based on the value of the clock on the SCK pin after a falling edge is detected on the chip select pin CSB.

Two configurations of the SPI interface are supported by the device: 4-wire and 3-wire. The protocol used by both configurations is the same. The device operates in the 4-wire configuration by default. It can be switched to 3-wire configuration by writing 0b1 to [IO_IF_CONF.spi_mode](#). In the 3-wire configuration, the pin SDX is used as the common bi-directional data pin.

The dedicated timing specifications for SPI of the device in addition to Table [1](#) are stated in Table [36](#). Figure [25](#) shows the definition of the SPI timings.

Table 36: SPI timings

Parameter	Comment	Symbol	Min	Typ	Max	Units
CSB lead time		T_setup_csb	40			ns
CSB lag time		T_hold_csb	40			ns
SDI setup time		T_setup_sdi	20			ns
SDI hold time		T_hold_sdi	20			ns
SDO output delay time	Load = 30pF	T_delay_sdo			30	ns
SDO release delay time	Load = 30pF	T_release_sdo			30	ns
SDO drive delay time	Load = 30pF	T_drive_sdo			30	ns
SCX pulse high time		T_high_scx	45			ns
SCX pulse low time		T_low_scx	45			ns

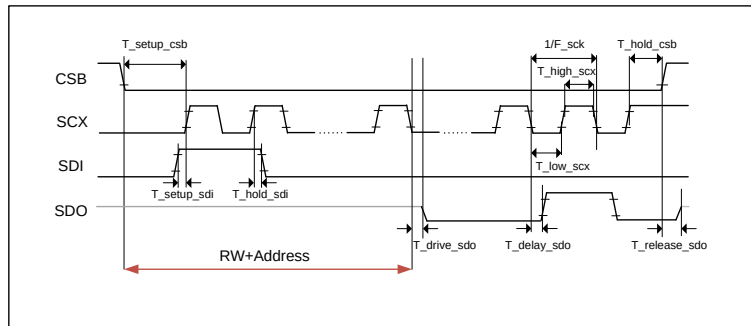


Figure 25: SPI timing diagram

SPI 4-wire protocol is based on the following pins:

- CSB (chip select low active)
- SCx (as SCK for serial clock)
- SDx (as SDI for serial data input)
- SDO (serial data output)

The communication starts when CSB is pulled low by the SPI controller and stops when CSB is pulled high again. SCK is also controlled by SPI controller. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

Multiple and single write operations are possible by keeping CSB low and continuing the data transfer. Only the address of the first register has to be sent via SDX. Addresses are automatically incremented² after each write access as long as CSB stays active low. The principle of multiple write is shown in Figure 26.

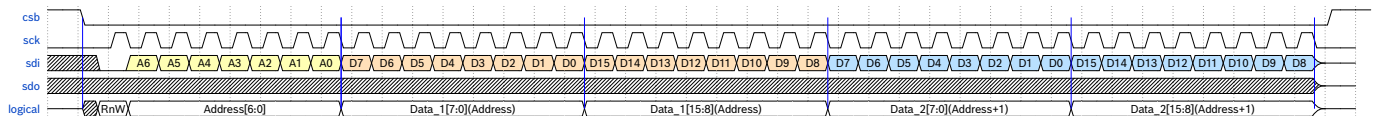


Figure 26: Multiple word write with the SPI protocol (4-wire)

The basic read operation waveform for 4-wire configuration is depicted in Figure 27. Please note, that the first two bytes received from the device via the SDO line correspond to dummy bytes and the 3rd byte corresponds to the value read out of the specified register address. That means, for a basic read operation, at least three bytes have to be read and the first two bytes have to be dropped and all following bytes can be interpreted.

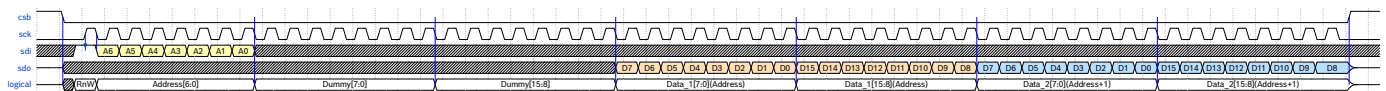


Figure 27: Multiple word read with the SPI protocol (4-wire)

- Address [A6-A0]: address of the first register
- Data $k[7:0]$, Data $k[15:8]$: when in write mode, these are the data via the SDI, which will be written into the address.
- Data $k[7:0]$, Data $k[15:8]$: when in read mode, these are the data on the SDO, which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low. Please note that the first two bytes received from the device via the SDO line correspond to dummy bytes and the 3rd byte corresponds to the value read out of the specified register address. The successive bytes read out correspond to values of incremented register addresses. That means, for a multiple read operation of n bytes, $n+2$ bytes have to be read, the first two have to be dropped and the successive bytes must be interpreted.

²Details on automatic address increment can be found in subsection 6.3.2

SPI 3-wire protocol is based on the following pins:

- CSB (chip select low active)
- SCx (as SCK for serial clock)
- SDx (serial data input and output)

SCK is controlled by the SPI controller. While SCK is pulled high, the communication starts when the CSB is pulled low by the SPI controller and stops when CSB is pulled high again. SDX is driven (when used as input of the device) at the falling edge of SCK and should be captured, when used as the output of the device, at the rising edge of SCK.

In a 3-wire configuration, the protocol as such is the same as in a 4-wire configuration. The basic operation for read and write access for 3-wire configuration is depicted in Figures 28 and 29, respectively.

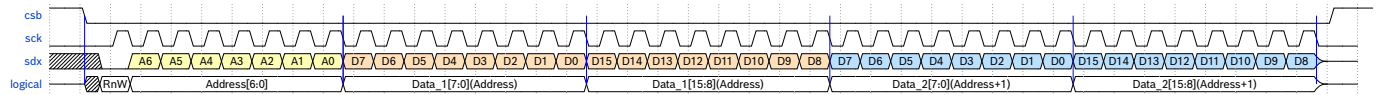


Figure 28: Multiple word write with the SPI protocol (3-wire)

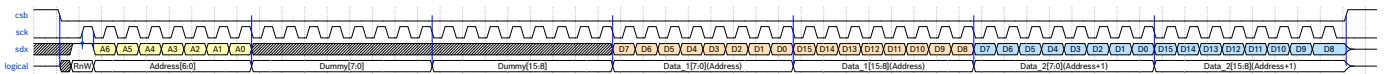


Figure 29: Multiple word read with the SPI protocol (3-wire)

6.2.3 I3C Protocol

The device supports the MIPI Improved Inter Integrated Circuit (I3C)³ protocol with the features:

- I3C single data rate (SDR) mode with up to 12.5 MHz data rate
- I²C compatibility, see Subsection 6.2.4
- In-Band Interrupt (IBI)
- Timing control (TC) modes:
 - Asynchronous (TC Async) mode 0 and mode 1

The I3C bus uses the pin SCX as SCL for serial clock and SDX as SDA for serial data input and output for the signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free.

The I3C interface of the device is compatible with the Improved Inter Integrated Circuit (I3C) Version 1.1.1 from 11 June 2021, and the Frequently Asked Questions (FAQ) for I3C Version 1.1 from 22 August 2022 available at <http://www.mipi.org/specifications/i3c-sensor-specification>.

The protocol used on the serial interface for writing data to the device consists of

- write the address byte, and
- then write instantly a sequence of words consisting of two bytes each.

The protocol used on the serial interface for reading data from the device consists of

- write the address byte, and then
- read:
 - two dummy bytes preceding the actual payload, and then instantly
 - the number of desired payload bytes/words.

The timing specification for I3C can be retrieved from the specification referred to above.

6.2.3.1 Bus Configuration

The I3C protocol uses several identifiers and codes to handle communication between several controllers and targets. For communication with this device, there are defined

- the provisional ID,

³I3C and MIPI are trademarks of MIPI Alliance.

- the Device Characteristics Register (DCR),
- the Bus Characteristics Register (BCR), and
- the Mandatory Byte (MDB) for IBIs.

The provisional ID has the value defined as detailed in in Table 37, which defaults to 0x0770'10AB'0001 with SDO=GND, where

- Bit 12 is controlled by the level on the SDO pin during power on reset, that is GND for 0b0 and VDDIO for 0b1
- Bit 13 to 15 are the so-called instance ID and defined as "0b000".

Table 37: Provisional Identifier

Byte	Byte 5								Byte 4								Byte 3								Byte 2								Byte 1								Byte 0								
Bit of byte	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Bit of word	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
De-scription	MIPI member ID																IDT	Bosch group ID				Device ID								Instance ID				Reserved															
Bit value	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	0	SDO	0	0	0	0	0	0	0	0	0	0	0	1
Hex value	0				7				7				0				1				0				A				B				0 or 1				0				0				1				

The value of the Device Characteristics Register (DCR) is fixed to 0x44. The value of the Bus Characteristics Register (BCR) is fixed to 0x26. This has the following meanings:

- Bit 5 of the BCR is set to 0b0, that is the device supports solely SDR.
- Bit 2 of the BCR is set to 0b1, that means that an accepted IBI is followed by the so-called mandatory byte.

For details on the mandatory byte, please refer to the IBI description in the paragraph [In-Band Interrupt](#).

The timing requirement is defined in Table 122 "I3C Open Drain Timing Parameters" and Table 123 "I3C Push-Pull Timing Parameters for SDR, ML, HDR-DDR, and HDR-BT Modes" in the I3C specification "Improved Inter Integrated Circuit Version 1.1.1 – 11 June 2021".

Address Range The controller can assign Dynamic Addresses from the allowed set of values to the device, with exceptions as defined in the I3C Target Address Restrictions in Table 8 in section 5.1.2.2.5 of the I3C specification "Improved Inter Integrated Circuit Version 1.1.1 – 11 June 2021".

6.2.3.2 Read and Write Access

The SDR read and write access follows the I3C specification. In the following, examples are given for write operations with Tables 38 and 39 for single-word and multi-word writes and for read operations with Tables 40 and 41 for single-word and multi-word reads, respectively. On multi-word access the register addresses are automatically incremented⁴. For the diagrams/tables, the following color coding is applied:

- transfer from the host to the device is indicated by greenish colored normal text
- transfer from the device to the host is indicated by orange colored text in italics
- acknowledgment from the device to the host:
 - with hand-off is indicated by orange colored text in italics
 - without hand-off is indicated by brown colored text in italics
- drives from either host or device are indicated by magenta bold text.

⁴Details on automatic address increment can be found in subsection [6.3.2](#)

In the diagrams, these abbreviations are used:

S Start

Sr Repeated start

P Stop

ACK Acknowledge

T Transition

For the examples of reading data from the device in Tables 40 and 41, the stop (P) can be removed and replaced by a repeated start (Sr).

Table 38: I3C Single-Word Write Operation

Broadcast Address		Specified Target DAA		Register N Address	Register N Data [7:0]	Register N Data [15:8]	
S	7'h7E+'0'	ACK	Sr	7'hDAA+'0'	ACK	Address N	T Data N low byte T Data N high byte T P/Sr

Table 39: I3C Multi-Word Write Operation

Broadcast Address		Specified Target DAA		Register M Address	Register M Data [7:0]	Register M Data [15:8]	...
S	7'h7E+'0'	ACK	Sr	7'hDAA+'0'	ACK	Address M	T Data M low byte T Data M high byte T ...
	...	Register N-1 Data [7:0]		Register N-1 Data [15:8]	Register N Data [7:0]	Register N Data [15:8]	
	...	Data N-1 low byte	T	Data N-1 high byte	T Data N low byte	T Data N high byte	T P/Sr

Table 40: I3C Single-Word Read Operation (Non-Repeated Start)

Broadcast Address		Specified Target DAA		Register N Address	
S	7'h7E+'0'	ACK	Sr	7'hDAA+'0'	ACK Address N T P

Broadcast Address		Specified Target DAA		dummy byte		dummy byte	...
S	7'h7E+'0'	ACK	Sr	7'hDAA+'1'	ACK	0x00	T 0x00 T ...

...	Register N Data [7:0]	Register N Data [15:8]	
...	Data N low byte	T Data N high byte	T P/Sr

Table 41: I3C Multi-Word Read Operation (Non-Repeated Start)

Broadcast Address		Specified Target DAA		Register M Address	
S	7'h7E+'0'	ACK	Sr	7'hDAA+'0'	ACK Address M T P

Broadcast Address		Specified Target DAA		dummy byte		dummy byte	...
S	7'h7E+'0'	ACK	Sr	7'hDAA+'1'	ACK	0x00	T 0x00 T ...

...	Register M Data [7:0]	Register M Data [15:8]	...
...	Data M low byte	T Data M high byte	T ...
...	Register N-1 Data [7:0]	Register N-1 Data [15:8]	...
...	Data N-1 low byte	T Data N-1 high byte	T ...

...	Register N Data [7:0]	Register N Data [15:8]	
...	Data N low byte	T Data N high byte	T P/Sr

6.2.3.3 Controller Clock Stalling

The I3C specification defines controller clock stalling. This allows the controller to stall the clock for at most 100 μ s. This is fully supported by the device according to the I3C specification.

6.2.3.4 In-Band Interrupt

The device supports the IBI feature as defined in the section 5.1.6.2 of the I3C specification “Improved Inter Integrated Circuit Version 1.1.1 – 11 June 2021”.

The feature is enabled by default after power-up and a subsequent execution of the Dynamic Address Assignment (DAA). If DAA is reset via the Common Command Code (CCC) Reset Dynamic Address Assignment (RSTDAA), the issuing of IBI will be disabled automatically. As long as no new dynamic address has been assigned, IBIs will stay disabled and must be enabled explicitly by the CCC ENEC in contrast to the situation after power-up. The IBI feature can be enabled by the ENEC CCC with the ENINT bit set to 0b1, and can be disabled by the DISEC CCC with the DISINT bit set to 0b1.

Raising in-band interrupts by the target has the following scheme: if no START is forthcoming within the Bus Available Condition, the chip will actively pull down the SDA line to issue a START. In case there is an IBI event, the device will emit its address into the arbitrated address header following a START (but not following a repeated START).

The device specific IBI payload format is defined in Table 42 and Table 43 depending on enabled TC Async modes. By retrieving both additional IBI payload bytes, the register `INT_STATUS_IBI` gets cleared automatically.

Table 42: In-band Interrupt Payload Format

TC configuration	Byte No.	Name	Bit	Description
No TC Async	1	MDB	[7:5]	Interrupt Group Identifier fixed to 0x0
			[4:0]	Interrupt status bits or'ed according to Table 43
	2	Additional Byte 1	[7:0]	LSB content of <code>INT_STATUS_IBI</code>
	3	Additional Byte 2	[15:8]	MSB content of <code>INT_STATUS_IBI</code>
TC Async 0	1	MDB	[7:5]	Interrupt Group Identifier fixed to 0x4
			[4:0]	Interrupt status bits or'ed according to Table 43
	2	T_C1_LSByte	[7:0]	LSByte of Target C1 counter value
	3	T_C1_MSByte	[7:0]	MSByte of Target C1 counter value
	4	T_C2	[7:0]	Target C2 counter value
	5	Additional Byte 1	[7:0]	LSB content of <code>INT_STATUS_IBI</code>
	6	Additional Byte 2	[15:8]	MSB content of <code>INT_STATUS_IBI</code>
TC Async 1	1	MDB	[7:5]	Interrupt Group Identifier fixed to 0x4
			[4:0]	Interrupt status bits or'ed according to Table 43
	2	T_C1_LSByte	[7:0]	LSByte of Target C1 counter value
	3	T_C1_MSByte	[7:0]	MSByte of Target C1 counter value
	4	T_C2	[7:0]	Target C2 counter value
	5	T_aBE	[7:0]	Target aBE counter value
	6	Additional Byte 1	[7:0]	LSB content of <code>INT_STATUS_IBI</code>
	7	Additional Byte 2	[15:8]	MSB content of <code>INT_STATUS_IBI</code>

Table 43: I3C Mandatory Data Byte Format

Bit	Purpose	Description
0	Specific Interrupt Identifier Field	FIFO Watermark IRQ or'ed with FIFO full IRQ
1		Sample ready IRQs (DRDY) of acceleration, angular rate and temperature or'ed
2		All feature IRQs or'ed
3		0b0
4		Low Power Wake Up (LPWUP)
5	Interrupt Group Identifier	Depending on TC Async Configuration:
6		▪ No TC Async enabled: 0x00
7		▪ TC Async 0/1 enabled: 0x04

6.2.3.5 I3C Timing Control

The device supports timing control modes as defined by the I3C standard. As defined by the specification, the device supports timing control for asynchronous systems and events called asynchronous modes (TC Async) . The modes can be configured, entered, and left using common command codes (CCCs).

Modes for Asynchronous Systems and Events The device supports the asynchronous modes 0 and 1 of TC Async as defined in the specification. Entering and leaving the asynchronous modes follows the specification. For entering the asynchronous mode 0, the host sends the CCC SETXTIME with the defining byte 0xDF, for asynchronous mode 1 the defining byte has to be set to 0xEF. For exiting any timing control mode, the host sends the CCC SETXTIME with sub-command 0xFF. The additional IBI payload bytes for the asynchronous modes are detailed in Table 42.

6.2.3.6 Common Command Codes

Table 44 lists the I3C Common Command Codes (CCC) supported by the device.

Table 44: Supported I3C Common Command Codes

CCC Code	CCC Type	MIPI Requires	CCC name	Description	Supported
0x00 / 0x80	Broadcast / Direct	Y	ENEC	enable events command	Y
0x01 / 0x81	Broadcast / Direct	Y	DISEC	disable events command	Y
0x02...0x05 / 0x82...0x85	Broadcast / Direct	N	ENTAS0 ... ENTAS3	enter activity state 0-3	N
0x06 / 0x86	Broadcast / Direct	Y / N ⁵	RSTDAA	reset dynamic address assignment	Y / N
0x07	Broadcast	Y	ENTDAA	enter dynamic address assignment	Y
0x09 / 0x89	Broadcast / Direct Set	N ⁶	SETMWL	set max write length	N
0x0A / 0x8A	Broadcast / Direct Set	Y	SETMRL	set max read length	Y
0x0B	Broadcast	N	ENTTM	enter test mode	N
0x20...0x27	Broadcast	N	ENTHDR0 ... ENTHDR7	enter HDR mode 0 - 7	N ⁷
0x28 / 0x98	Broadcast / Direct	N	SETXTIME	exchange timing information	Y
0x29	Broadcast	N	SETAASA	set all addresses to static addresses	Y
0x2A / 0x9A	Broadcast / Direct	Y	RSTACT	target reset action	Y
0x2E...0x60	Broadcast	N		MIPI reserved	N
0x61...0x7F	Broadcast	N		vendor extension - broadcast CCCs	N
0x87	Direct Set	N	SETDASA	set dynamic address assignment from static address	Y ⁸
0x88	Direct Set	Y	SETNEWDA	set new dynamic address	Y
0x8B	Direct Get	Y	GETMWL	get max write length	Y
0x8C	Direct	Y	GETMRL	get max read length	Y
0x8D	Direct	Y	GETPID	get provisional ID	Y
0x8E	Direct	Y	GETBCR	get bus characteristics register	Y
0x8F	Direct	Y	GETDCR	get device characteristics register	Y
0x90	Direct Get	Y	GETSTATUS	get device status	Y
0x94	Direct Get	N	GETMXDS	get max data speed	N
0x95	Direct Get	N	GETCAPS	get HDR capability	Y
0x99	Direct	N	GETXTIME	get timing information	Y
0x9E...0xDF	Direct	N		MIPI reserved	N
0xE0...0xFE	Direct	N		vendor extension - direct CCCs	N

Support for Defining Byte Defining Byte formats for the following CCCs are not supported and will always respond with a fixed format:

- GETSTATUS with format 1 (defined by GETCAP3[4] = 0b0) returning 2 bytes
- GETCAPS with format 1 (defined by GETCAP3[3] = 0b0) returning 4 bytes

⁵deprecated CCC

⁶These features are optional for the target, see section 5.1.9.3.5 "Set/Get Max Write Length" in the I3C specification "Improved Inter Integrated Circuit Version 1.1.1 – 11 June 2021".

⁷ENTHDRx CCCs are recognized, but the device does not support HDR operations.

⁸The device does not support SETDASA Format 2: Point-to-Point

Details on Direct Get CCCs

GETCAPS (Get Optional Feature Capabilities) format 1 returns the four bytes listed in Table 45.

Table 45: GETCAPS Returning Value

Byte No.	Byte	Bit	Name	Description
1	GETCAP1	[7:0]	High Data Rate (HDR) Mode	No HDR supported
2	GETCAP2	[7:6] = 0b0	Defining Byte Support	Not supported
		[5:4] = 0b0	Group Address Capabilities	Not supported
		[3:0] = 0x1	I3C 1.x Specification Version	Minor version number of the I3C Specification
3	GETCAP3	[7] = 0b0	Reserved	
		[6] = 0b0	Pending Read Notification	No Pending Read Notification for IBI
		[5] = 0b0	HDR-BT CRC32 Support	Not supported
		[4:3] = 0b0	Defining Byte Support	No Defining Byte support for GETCAPS and GETSTATUS
		[2:1] = 0b0	Device to Device Transfer	Not supported
		[0] = 0b0	Multi-Lane for Speed Support	Not supported
4	GETCAP4	[7:0]=0x00	Reserved	

GETSTATUS (Get Device Status) format 1 returns the following two bytes in Table 46.

Table 46: GETSTATUS Returning Value

Bits	Name	Description
[15:8]	Status register	Provides bits[0:7] of the STATUS register
[7]	Activity mode	Gyroscope enabled status. Reads a 0b1 if gyroscope power operation state is other than Off
[6]	Activity mode	Accelerometer enabled status. Reads a 0b1 if accelerometer power operation state is other than Off
[5]	Protocol Error	If 1'b1: The device detected a protocol error since the last status read. The device might or might not be able to check for such errors. Note that this value self-clears upon every successful completion of a host read of the device's status.
[4] = 0b0	Reserved	
[3:0]	Pending Interrupt	Contains the interrupt number of any pending interrupt, or 0 if no interrupts are pending. If more than one interrupt is set, then the highest priority interrupt (highest value) is returned. The priorities of the interrupts are given in Table 47.

Table 47: GETSTATUS Pending Interrupt Priorities

Priority value	Interrupt Name
0x0F	FIFO_full or FIFO_wm
0x0E	OIS DRDY
0x0D	-
0x0C	GYR_DRDY
0x0B	ACC_DRDY
0x0A	TEMP_DRDY
0x09	LPWUP
0x08	Feature interrupts according to bits[8:15] from INT_STATUS_IBI in reversed order: bit15 corresponds to a value of 0x01
0x07	
0x06	
0x05	
0x04	
0x03	
0x02	
0x01	
0x00	None

GETMWL (Get Max Write Length) returns the two bytes outlined in Table 48.

Table 48: GETMWL Returning Value

Byte No.	Byte	Bit	Name	Description
1	MWL MSB	[7:0] = 0xFF	MSByte of Max Write Length	No limit
2	MWL LSB	[7:0] = 0xFF	LSByte of Max Write Length	

GETMRL (Get Max Read Length) returns the three bytes in Table 49.

Table 49: GETMRL Returning Value

Byte No.	Byte	Bit	Name	Description
1	MRL MSB	[7:0] = 0xFF	MSByte of Max Read Length	No limit
2	MRL LSB	[7:0] = 0xFF	LSByte of Max Read Length	
3	IBI PL	[7:0]	IBI Payload Size	Values: (also see Table 42) 0x03: When No TC is activated. IBI payload size is 3 bytes, including MDB + 2 additional bytes. 0x06: When TC Async 0 is activated. IBI payload size is 6 bytes, including MDB + 4 additional bytes. 0x07: When TC Async 1 is activated. IBI payload size is 7 bytes, including MDB + 5 additional bytes.

GETXTIME (Get Exchange Timing Support Information) returns the following four bytes in Table 50.

Table 50: GETXTIME Returning Value

Byte No.	Name	Description
1	Supported Modes Byte	TC Async 0 and TC Async 1 are supported.
2	State Byte	TC Async 0 and TC Async 1 enabling state is shown. Overflow bit is related to Async Mode 0 and 1.
3	Frequency Byte	depends on trim value
4	Inaccuracy Byte	depends on trim value

The overflow bit in Byte No. 2 will be set in case any TC Async counter overflows, and will be cleared automatically in the following way:

- TC Async 0: a new IBI is requested by hardware interrupt.
- TC Async 1: an I3C start has been found after a drdy event.

Note that the overflow bit will not be cleared by the GETXTIME.

6.2.4 I²C Protocol

The device supports the following I²C modes:

- Standard mode (Sm) (100 kHz)
- Fast mode (Fm) (400 kHz)
- Fast mode plus (Fm+) (1 MHz)

The default I²C legacy address of the device is 7h'0b1101000 (0x68). It is used if the SDO pin is pulled to 'GND' during power-up. The alternative address 7h'0b1101001 (0x69) is selected by pulling the SDO pin to 'VDDIO' during power-up. After power-up the address is fixed and can only be changed by a power-cycle or soft-reset. Only the 7-bit address mode is supported.

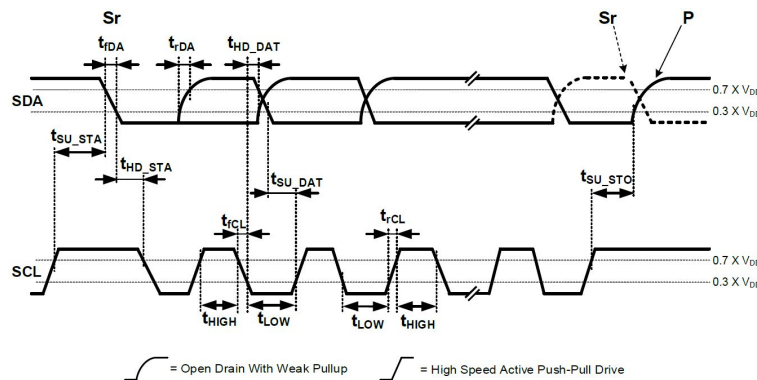
The I²C interface of the device is compatible with the legacy support of I²C of the standard "I3CSM Improved Inter Integrated Circuit Version 1.1.1" from 11 June 2021, and the "Frequently Asked Questions (FAQ) for MIPI I3CSM Version 1.1" from 22 August 2022 available at <http://www.mipi.org/specifications/i3c-sensor-specification>. The timing specification and diagrams for I²C can be retrieved from this specification. The I²C protocol uses the same pin configuration and sequences for writing and reading data as for I3C, as described in section 6.2.3.

The I²C timing requirements table and I²C Legacy Mode Timing diagram in Table 51 on the following page and Fig 30 on the next page are Copyright 2016 by MIPI Alliance, Inc. and reprinted with their permission⁹

⁹This material may not be disclosed, reproduced or used for any purpose other than as needed to support the use of the products of Bosch Sensortec GmbH. MIPI provides all such material on an AS IS basis, without warranty of any kind.

Table 51: I²C timings

Parameter	Symbol	100kHz / Sm		400kHz / Fm		1MHz / Fm+		Units
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	0.1	0	0.4	0	1.0	MHz
Setup time for a repeated START	$t_{SU,STA}$	4700	–	600	–	260	–	ns
Hold time for a (repeated) START	$t_{HD,STA}$	4000	–	600	–	260	–	ns
SCL clock low period	t_{LOW}	4700	–	1300	–	500	–	ns
	$t_{DIG,L}$	$t_{LOW} + t_{rCL}$	–	$t_{LOW} + t_{rCL}$	–	$t_{LOW} + t_{rCL}$	–	ns
SCL clock high period	t_{HIGH}	4000	–	600	–	260	–	ns
	$t_{DIG,H}$	$t_{HIGH} + t_{rCL}$	–	$t_{HIGH} + t_{rCL}$	–	$t_{HIGH} + t_{rCL}$	–	ns
Data setup time	$t_{SU,DAT}$	250	–	100	–	50	–	ns
Data hold time	$t_{HD,DAT}$	–	–	–	–	–	–	ns
SCL signal rise time	t_{rCL}	–	1000	20	300	–	120	ns
SCL signal fall time	t_{fCL}	–	300	$20 \cdot \left(\frac{V_{DDIO}}{5.5V}\right)$	300	$20 \cdot \left(\frac{V_{DDIO}}{5.5V}\right)$	120	ns
SDA signal rise time	t_{rDA}	–	1000	20	300	–	120	ns
SDA signal fall time	t_{fDA}	–	300	$20 \cdot \left(\frac{V_{DDIO}}{5.5V}\right)$	300	$20 \cdot \left(\frac{V_{DDIO}}{5.5V}\right)$	120	ns
Setup time for STOP	$t_{SU,STO}$	4000	–	600	–	260	–	ns
Bus free time between a STOP condition and a START condition	t_{BUF}	4.7	–	1.3	–	0.5	–	μ s
Pulse width of spikes that the spike filter must suppress	t_{SPIKE}	0	50	0	50	0	50	ns

Figure 30: I²C timing diagram

The I²C legacy protocol works as follows:

START: Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by I²C bus controller). Once the START signal is transferred by the controller, the bus is considered busy.

STOP: Each data transfer should be terminated by a Stop signal (P) generated by controller. The STOP condition is a low to high transition on SDA line while SCL is held high.

ACKNOWLEDGE: Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

A START immediately followed by a STOP (without SCL toggling from 'VDDIO' to 'GND') is not supported. If such a combination occurs, the STOP is not recognized by the device. In the following diagrams/tables, these abbreviations are used:

S Start

P Stop

ACK Acknowledge

RW Read / Write

In the diagrams/tables, a transfer from the host to the device is indicated by greenish coloured normal text while transfer from the device to the host is indicated by orange coloured text in italics.

I²C write access I²C write access can be used to write a data word in one sequence.

The sequence begins with start condition generated by the controller, followed by 7 bits target address and a write bit (RW = 0). The target sends an acknowledge bit (ACK = 0) and releases the bus. Then the controller sends the one byte register address. The target again acknowledges the transmission and waits for the two times 8 bits of data which shall be written to the specified register address. After the target has acknowledged the data bytes, the controller generates a stop signal and terminates the writing protocol. An example of an I²C write access is stated in Table 52.

Table 52: I²C Single-Word Write Operation

Start	Target Address	RW	ACK	Register M Address (0x38)	ACK	Register M Data [7:0]	ACK	Register M Data [15:8]	ACK	Stop
S	1101000	0	0	X0111000	0	11010101	0	00101010	0	P

Multi-word writes are supported without restriction on normal registers with auto-increment as well as on special registers with address stalling¹⁰. An example of an I²C multi-word write access is stated in Table 53.

Table 53: I²C Multi-Word Write Operation

Start	Target Address	RW	ACK	Register M Address (0x38)	ACK	Register M Data [7:0]	ACK	Register M Data [15:8]	ACK	
S	1101000	0	0	X0111000	0	11010101	0	00101010	0	┐

	Register N Data [7:0]	ACK	Register N Data [15:8]	ACK	Stop
L	10101010	0	01010101	0	P

I²C read access I²C read access can be used to read one or multiple data bytes or words in one sequence.

A read sequence consists of a one-byte I²C write phase followed by the I²C read phase to read a single byte, a single 16bit word of two bytes or multiple 16bit words. The two parts of the transmission must be separated by a repeated start condition (S). The I²C write phase addresses the target and sends the register address to be read. After target acknowledges the transmission, the controller generates again a start condition and sends the target address together with a read bit (RW = 1). Then, the controller releases the bus and waits for the data bytes to be read out from the target. The first two transmitted bytes are dummy bytes and have to be dropped. Then the target transmits the data of the requested address. After each byte transmitted by the target, the controller has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A non-ACK by the controller (NACK) (ACK = 1) stops the data being transferred from the target. The target releases the bus so that the controller can generate a STOP condition and terminate the transmission. The register address is automatically incremented¹⁰ and, therefore, more than one word can be read out sequentially. Once a new data read transmission starts, the start address will be set to the register address specified since the latest I²C write command. By default the start address is set at 0x00. In this way repetitive reads of words from the same starting address are possible. An example of an I²C single-word read access with Repeated Start is provided in Table 54.

¹⁰Details on automatic address increment can be found in subsection 6.3.2

Table 54: I²C Single-Word Read Operation

Start	Target Address	RW	ACK	Register N Address (0x33)	ACK
S	1101000	0	0	X011001	0

Start	Target Address	RW	ACK	dummy byte	ACK	dummy byte	ACK	
Sr	1101000	1	0	0000000	0	0000000	0	┐

	Register N Data [7:0]	ACK	Register N Data [15:8]	ACK	Stop
L	x x x x x x x x	0	x x x x x x x x	1	P

A further example of an I²C single byte read access with Repeated Start is provided in Table 55.

Table 55: I²C Single Byte Read Operation

Start	Target Address	RW	ACK	Register N Address (0x38)	ACK
S	1101000	0	0	X011100	0

Start	Target Address	RW	ACK	dummy byte	ACK	dummy byte	ACK	
Sr	1101000	1	0	0000000	0	0000000	0	┐

	Register N Data [7:0]	ACK	Stop
L	x x x x x x x x	1	P

An example of an I²C read access for multiple words with Repeated Start is given in Table 56.

Table 56: I²C Multi-Word Read Operation (with Repeated Start)

Start	Target Address	RW	ACK	Register M Address (0x33)	ACK
S	1101000	0	0	X011001	0

Start	Target Address	RW	ACK	dummy byte	ACK	dummy byte	ACK	
Sr	1101000	1	0	0000000	0	0000000	0	┐

	Register M Data [7:0]	ACK	Register M Data [15:8]	ACK	...
L	x x x x x x x x	0	x x x x x x x x	0	...

...	Register N Data [7:0]	ACK	Register N Data [15:8]	ACK	Stop
...	x x x x x x x x	0	x x x x x x x x	0	P

6.3 Digital communication

6.3.1 Communication Access Restriction

In order to allow for the correct internal synchronization of data written to or read from the device, certain access restrictions apply for consecutive write accesses or a write/read sequence through the I³C and I²C interface as well as SPI. The required waiting period depends on the operation mode of the device: In any power operation state except for Deep-Suspend an interface idle time of at least 2 μ s is required, for Deep-Suspend mode an idle time of 100 μ s is required. In SPI protocol, this idle time has to be kept between two consecutive CSB pull-downs.

As illustrated in Figure 31, an interface idle time of at least 2 μ s is required following an operation when the device operates in any mode.

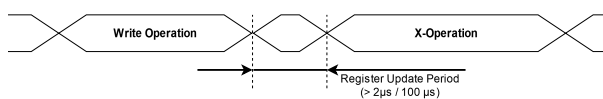


Figure 31: Post-Write Timing Constraints

6.3.2 Automatic Address Increment for Burst Access

Whenever a host accesses the device with a burst transfer, the register address is incremented upon each transmitted data word, independent of the access type (read or write). When the highest address (0x7F) is reached, it stays at this address (no wrap-around). On dedicated register addresses, the auto-incrementing is stalled, and all succeeding bytes are transferred with this stalled address. Auto-incrementing is stalled, even when the address is not the first one within a burst access. These stalling register addresses are:

- **FIFO_DATA** (read access only)
- **FEATURE_DATA_RX** (read access only)
- **FEATURE_DATA_TX** (write access only)

Note: The increment also includes reserved or unused register addresses. This should be avoided to prevent potentially undesired write-accesses or returning unspecified values.

7 Memory Map

The device can be operated through writes and reads of memory spaces. For the physical sensing including data buffering via the primary logical interface, this is provided through a register file described in the register map in section 7.1. The configuration and extended outputs of the advanced and application features provided by the feature engine can be accessed through the extended register map. The layout of the extended registers is described in Section 7.2.

For all data read from registers, content marked as reserved must be ignored. If only the first byte of a register contains non-reserved data, the upper byte is not required to be read.

When performing an update of a register with fields marked as reserved (partial update), a read-modify-write approach has to be followed to write the content of a register. That means, for a write access to a register with reserved content, the whole register must be read, then the desired content must be updated and the content written (back) to the register to avoid overwriting the reserved part with undefined content. This is especially important for the extended register map where many configurations are located.

7.1 Register File Description

The description of the register file is split into the register map as overview and a detailed description for each register. The next section 7.1.1 provides an overview of the register file as map and section 7.1.2 explains details for all registers the fields with their purpose.

Some registers serve the dedicated purpose of controlling the feature engine. The usage of the related registers [FEATURE_STATUS_0](#) to [FEATURE_STATUS_3](#) and [FEATURE_IO_0](#) to [FEATURE_IO_2](#) together with the register [FEAT_ENG_SYNC](#) is explained in section 5.8. The memory access to the extended registers through the registers [FEATURE_DATA_CTRL](#), [FEATURE_DATA_RX](#) and [FEATURE_DATA_TX](#) is explained in section 7.2.

7.1.1 Register Map

Table 57 provides an overview of the register map of the device.

Table 57: Register Map Overview¹

Legend			Read-only				Read/Write				Write-only				Reserved			
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	CHIP_ID	0x00AB	reserved								chip_id							
...	-	-	reserved															
0x07	ERR_REG	0x0000	reserved		i3c_te5...	i3c_te4...	i3c_te3...	i3c_te2...	i3c_te1...	i3c_te0...	reserved	gyr_con...	acc_con...	reserved	nvm_pro...	reserved	gyr_err	fatal_err
0x08	STATUS	0x0082	reserved								por_det...	reserved		drdy_acc	drdy_gyr	reserved	cmd_rdy	reserved
0x09	ACC_DATA_X_LSB	0x0000	acc_x_15_0															
0x0A	ACC_DATA_X_MSB	0xFF80	acc_x_31_16															
0x0B	ACC_DATA_Y_LSB	0x0000	acc_y_15_0															
0x0C	ACC_DATA_Y_MSB	0xFF80	acc_y_31_16															
0x0D	ACC_DATA_Z_LSB	0x0000	acc_z_15_0															
0x0E	ACC_DATA_Z_MSB	0xFF80	acc_z_31_16															
0x0F	GYR_DATA_X_LSB	0x0000	gyr_x_15_0															
0x10	GYR_DATA_X_MSB	0xFF80	gyr_x_31_16															
0x11	GYR_DATA_Y_LSB	0x0000	gyr_y_15_0															
0x12	GYR_DATA_Y_MSB	0xFF80	gyr_y_31_16															
0x13	GYR_DATA_Z_LSB	0x0000	gyr_z_15_0															
0x14	GYR_DATA_Z_MSB	0xFF80	gyr_z_31_16															
0x15	TEMP_DATA	0x8000	temperature															
0x16	SENSORTIME_DATA_LSB	0x0000	sensortime_15_0															
0x17	SENSORTIME_DATA_MSB	0x0000	reserved								sensortime_23_16							
0x18	INT_STATUS_INT1	0x0000	cmd_exe...	reserved	vad_int1	activit...	www_wgd...	tap_det...	gen_int...	sd_scwm...	lp_wup...	fifo_fu...	fifo_wm...	reserved	drdy_te...	reserved	drdy_gy...	drdy_ac...
0x19	INT_STATUS_INT2	0x0000	cmd_exe...	reserved	vad_int2	activit...	www_wgd...	tap_det...	gen_int...	sd_scwm...	lp_wup...	fifo_fu...	fifo_wm...	reserved	drdy_te...	reserved	drdy_gy...	drdy_ac...
0x1A	INT_STATUS_IBI	0x0000	cmd_exe...	reserved	vad_ibi	activit...	www_wgd...	tap_det...	gen_int...	sd_scwm...	lp_wup_ibi	fifo_fu...	fifo_wm...	reserved	drdy_te...	reserved	drdy_gy...	drdy_ac...
0x1B	FEATURE_STATUS_0	0x0000	reserved							status_...	status_...	status_...	status_...	status_...	status_...	status_...	status_...	status_...
0x1C	FEATURE_STATUS_1	0x0000	reserved								detected_activity				wrist_gesture		status_ww_wakeup...	
0x1D	FEATURE_STATUS_2	0x0000	step_count_15_0															
0x1E	FEATURE_STATUS_3	0x0000	reserved											step_count_20_16				
0x1F	FEATURE_IO_0	0x0000	wrng_ac...	wrng_ac...	cmd_status	cmd_response				cmd_han...	cmd_response_feature						feat_eng_state	
0x20	FEATURE_IO_1	0x0000	dis_fea...	cond_usr2alt_switch				cond_alt2usr_switch				cmd_feature_select				reserved		

¹Long register and field names are abbreviated with '...'. When hovering over '...' most PDF viewers display the full name.

Table 57: Register Map Overview (continued)

Legend			Read-only				Read/Write				Write-only				Reserved							
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0				
0x21	FEATURE_IO_2	0x0000	reserved		en_vad	en_acti...	en_wg_d...	en_ww_w...	en_trip...	en_doub...	en_sing...	en_gen_...	en_gen_...	en_gen_...	en_gen_...	en_sig_...	en_step...	en_step...				
0x22	FEAT_ENG_SYNC	0x0000	reserved																feature...			
0x23	FIFO_FILL_LVL	0x0000	reserved				fifo_fill_lvl															
0x24	FIFO_DATA	0x8000	fifo_data																			
0x25	FILTER_CONF	0x0202	reserved				gyr_sat...	reserved	gyr_filter_type			reserved				acc_sat...	reserved	acc_filter_type				
0x26	ACC_CONF	0x0028	acc_mode			acc_avg_num			acc_bw			acc_range			acc_odr							
0x27	GYR_CONF	0x0058	gyr_mode			gyr_avg_num			gyr_bw			gyr_range			gyr_odr							
...	-	-	reserved																			
0x29	ALT_FILTER_CONF	0x0202	reserved						alt_gyr_filter_type		reserved						alt_acc_filter_type					
0x2A	ALT_ACC_CONF	0x0028	alt_acc_mode			alt_acc_avg_num			alt_acc_bw			alt_acc_range			alt_acc_odr							
0x2B	ALT_GYR_CONF	0x0058	alt_gyr_mode			alt_gyr_avg_num			alt_gyr_bw			alt_gyr_range			alt_gyr_odr							
0x2C	ALT_CONF	0x4000	alt_rst...	reserved						alt_gyr_en		reserved						alt_acc_en				
0x2D	ALT_STATUS	0x2424	reserved								alt_gyr...		reserved						alt_acc...			
0x2E	SELFTTEST_STATUS	0x0000	reserved				gyr_st_status		reserved								acc_st_status					
0x2F	HIF_CONFIG	0x0000	reserved																cor_config			
0x30	FIFO_WATERMARK	0x0000	reserved						fifo_watermark													
0x31	FIFO_CONF	0x0000	reserved		fifo_sensor_time		fifo_te...		reserved	fifo_gy...		fifo_ac...		reserved				fifo_en		fifo_st...		
0x32	FIFO_CTRL	0x0000	reserved																fifo_flush			
0x33	IO_INT_CTRL	0x0000	reserved						int2_ou...		int2_od	int2_lvl		reserved				int1_ou...		int1_od	int1_lvl	
0x34	INT_CONF	0x0000	reserved								int2_mode			reserved						int1_mode		
0x35	INT_MAP_HW	0x0000	lp_wup_int_map		fifo_full_int_map		fifo_wm_int_map		reserved		temp_drdy_int_map		reserved		gyr_drdy_int_map		acc_drdy_int_map					
0x36	INT_MAP_FEAT_ENG	0x0000	cmd_exe_map		reserved		vad_map		act_change_map		www_wgd_int_map		tap_int_map		gen_int_map		sd_schw_sigmoid_map					
0x37	LPWUP_EN	0x0000	reserved												lpwup_e...		lpwup_z_en		lpwup_y_en		lpwup_x_en	
0x38	LPWUP_CFG	0x0000	lpwup_dur			lpwup_ths																
0x39	LPWUP_STATUS	0x0000	reserved												lpwup_end		lpwup_z	lpwup_y		lpwup_x		
0x3A	FEAT_ENG_GLOB_CTRL	0x8000	reserved								wake_on...		reserved						feat_eng_mode			
0x3B	FEATURE_DATA_CTRL	0x0000	data_cmd		reserved		data_addr															
0x3C	FEATURE_DATA_TX	0x0000	data_tx_value																			
0x3D	FEATURE_DATA_RX	0x0000	data_rx_value																			
...	-	-	reserved																			
0x3F	FEAT_ENG_STATUS	0x0008	reserved						data_oo...		feature...	feature...	reserved			feat_en...		reserved		feat_en...		
...	-	-	reserved																			
0x49	IO_IF_CONF	0x0000	reserved																spi_mode			

Table 57: Register Map Overview (continued)

Legend			Read-only				Read/Write				Write-only				Reserved				
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
0x4A	IO_PAD_STRENGTH	0x0064	reserved			if_proto_force		reserved				i2c_boost		reserved			drv_str		
0x4B	IO_ODR_DEVIATION	0x0000	reserved											odr_deviation					
...	-	-	reserved																
0x54	LEG_ERR_REG	0x0000	reserved		leg_i3c...	leg_i3c...	leg_i3c...	leg_i3c...	leg_i3c...	leg_i3c...	reserved	leg_gyr...	leg_acc...	reserved	leg_nvm...	reserved	leg_gyr...	leg_fat...	
0x55	LEG_STATUS	0x0082	reserved								leg_por...		reserved		leg_drd...	leg_drd...	reserved	leg_cmd...	reserved
0x56	LEG_ACC_DATA_X	0x8000	leg_acc_x																
0x57	LEG_ACC_DATA_Y	0x8000	leg_acc_y																
0x58	LEG_ACC_DATA_Z	0x8000	leg_acc_z																
0x59	LEG_GYR_DATA_X	0x8000	leg_gyr_x																
0x5A	LEG_GYR_DATA_Y	0x8000	leg_gyr_y																
0x5B	LEG_GYR_DATA_Z	0x8000	leg_gyr_z																
0x5C	LEG_TEMP_DATA	0x8000	leg_temperature																
0x5D	LEG_SENSORTIME_DA...	0x0000	leg_sensortime_15_0																
0x5E	LEG_SENSORTIME_DA...	0x0000	reserved								leg_sensortime_23_16								
0x5F	SAT_FLAGS	0x0000	reserved											satf_gyr_z	satf_gyr_y	satf_gyr_x	satf_acc_z	satf_acc_y	satf_acc_x
0x60	GYR_GAIN_X	0x0000	reserved								gyr_gain_x								
0x61	GYR_GAIN_Y	0x0000	reserved								gyr_gain_y								
0x62	GYR_GAIN_Z	0x0000	reserved								gyr_gain_z								
...	-	-	reserved																
0x64	ACC_GAIN_X	0x0000	reserved								acc_gain_x								
0x65	ACC_GAIN_Y	0x0000	reserved								acc_gain_y								
0x66	ACC_GAIN_Z	0x0000	reserved								acc_gain_z								
...	-	-	reserved																
0x6A	GYR_OFFS_X	0x0000	reserved								gyr_offs_x								
0x6B	GYR_OFFS_Y	0x0000	reserved								gyr_offs_y								
0x6C	GYR_OFFS_Z	0x0000	reserved								gyr_offs_z								
...	-	-	reserved																
0x6E	ACC_OFFS_32G_X	0x0000	reserved								acc_offs_32g_x								
0x6F	ACC_OFFS_32G_Y	0x0000	reserved								acc_offs_32g_y								
0x70	ACC_OFFS_32G_Z	0x0000	reserved								acc_offs_32g_z								
0x71	ACC_OFFS_8G_X	0x0000	reserved								acc_offs_8g_x								
0x72	ACC_OFFS_8G_Y	0x0000	reserved								acc_offs_8g_y								
0x73	ACC_OFFS_8G_Z	0x0000	reserved								acc_offs_8g_z								
...	-	-	reserved																

Table 57: Register Map Overview (continued)

Legend			Read-only				Read/Write				Write-only				Reserved			
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x7B	LEGACY_CONF	0x0000	reserved															legacy_...
0x7C	PWR_CONF	0x0000	reserved															adv_pow...
...	-	-	reserved															
0x7E	CMD	0x0000	cmd															
...	-	-	reserved															

7.1.2 Register Map Details

Register (0x00) **CHIP_ID**

Description: CHIP identification code

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	1	0	1	0	1	1
Content	chip_id							

- reserved: do not interpret.
- chip_id: (bit offset: 0, bit width: 8, access: read-only) The product chip_id.
Following values can be read from the field chip_id:

Value	Description
0xAB	product identifier for BMI423

Use this link to go back to the overview table: [CHIP_ID](#).

Register (0x07) **ERR_REG****Description:** Reports sensor error conditions

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		i3c_te5...	i3c_te4...	i3c_te3...	i3c_te2...	i3c_te1...	i3c_te0...

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved	gyr_con...	acc_con...	reserved	nvm_pro...	reserved	gyr_err	fatal_err

- reserved: do not interpret; in case of write, provide the current value.
- fatal_err: (bit offset: 0, bit width: 1, access: read-only) Fatal Error, chip is not in operational state (Boot-failure). This flag will be reset only by power-on-reset or softreset.
Following values can be read from the field fatal_err:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- gyr_err: (bit offset: 1, bit width: 1, access: read-only) Gyroscope not operational due to error conditions. This flag will be cleared if gyro is configured to DISABLE by the user.
Following values can be read from the field gyr_err:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- nvm_prog_err: (bit offset: 3, bit width: 1, access: read-only) The command NVM_PROG failed. Bit is reset with next NVM_PROG command.
Following values can be read from the field nvm_prog_err:

Value	Description
0b0 (0x0) (default)	No error during NVM_PROG command execution
0b1 (0x1)	Error during NVM_PROG command execution

- acc_conf_err: (bit offset: 5, bit width: 1, access: read-only) Unsupported accelerometer configuration set by user. This flag will be reset when configuration has been corrected.
Following values can be read from the field acc_conf_err:

Value	Description
0b0 (0x0) (default)	accel sensor configuration okay
0b1 (0x1)	accel sensor configuration invalid

- gyr_conf_err: (bit offset: 6, bit width: 1, access: read-only) Unsupported gyroscope configuration set by user. This flag will be reset when configuration has been corrected.

Following values can be read from the field `gyr_conf_err`:

Value	Description
0b0 (0x0) (default)	gyro sensor configuration okay
0b1 (0x1)	gyro sensor configuration invalid

- `i3c_te0_err`: (bit offset: 8, bit width: 1, access: read-write) Invalid Broadcast Address/W (7'h7E/W) or Dynamic Address/RnW after DA assignment Detect any of the following: 7'h3E / W 7'h5E / W 7'h6E / W 7'h76 / W 7'h7A / W 7'h7C / W 7'h7F / W 7'h7E / R This flag is clear-on-read

Following values can be set to or read from the field `i3c_te0_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `i3c_te1_err`: (bit offset: 9, bit width: 1, access: read-write) CCC Code; Parity Check, using T-Bit; This flag is clear-on-read

Following values can be set to or read from the field `i3c_te1_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `i3c_te2_err`: (bit offset: 10, bit width: 1, access: read-write) Write Data; Parity Check, using T-Bit; This flag is clear-on-read

Following values can be set to or read from the field `i3c_te2_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `i3c_te3_err`: (bit offset: 11, bit width: 1, access: read-write) Assigned Address during Dynamic Address Arbitration; Parity Check, using T-Bit; This flag is clear-on-read

Following values can be set to or read from the field `i3c_te3_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `i3c_te4_err`: (bit offset: 12, bit width: 1, access: read-write) 7'h7E/R missing after Sr during Dynamic Address Arbitration; Detect 7'h7E/R missing after Sr during Dynamic Address Arbitration This flag is clear-on-read

Following values can be set to or read from the field `i3c_te4_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `i3c_te5_err`: (bit offset: 13, bit width: 1, access: read-write) Transaction after detecting CCC; Detect illegally formatted CCC; This flag is clear-on-read
Following values can be set to or read from the field `i3c_te5_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

Use this link to go back to the overview table: [ERR_REG](#).

Register (0x08) **STATUS****Description:** Sensor status flags

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R	R	R/W	R/W	R	R	R
Reset Value	1	0	0	0	0	0	1	0
Content	por_det...	reserved		drdy_acc	drdy_gyr	reserved	cmd_rdy	reserved

- reserved: do not interpret; in case of write, provide the current value.
- cmd_rdy: (bit offset: 1, bit width: 1, access: read-only) CMD decoder status.
Following values can be read from the field cmd_rdy:

Value	Description
0b0 (0x0)	Command in progress.
0b1 (0x1) (default)	Command decoder is ready to accept a new command.

- drdy_gyr: (bit offset: 3, bit width: 1, access: read-write) Data ready for Gyroscope. It gets reset, when STATUS register is read out
- drdy_acc: (bit offset: 4, bit width: 1, access: read-write) Data ready for Accelerometer. It gets reset, when STATUS register is read out
- por_detected: (bit offset: 7, bit width: 1, access: read-write) Flag is set only after POR. It gets reset, when STATUS register is read out

Use this link to go back to the overview table: [STATUS](#).

Register (0x09) **ACC_DATA_X_LSB****Description:** Acceleration sample, X axis LSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	acc_x_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	acc_x_15_0							

- **acc_x_15_0:** (bit offset: 0, bit width: 16, access: read-only) Acceleration X axis LSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, the saturation flag is encoded here into the LSB (bit 0). The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_DATA_X_LSB](#).

Register (0x0A) **ACC_DATA_X_MSB****Description:** Acceleration sample, X axis MSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	1	1	1	1	1	1	1
Content	acc_x_31_16							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	acc_x_31_16							

- acc_x_31_16: (bit offset: 0, bit width: 16, access: read-only) Acceleration X axis MSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, please handle correctly the saturation flag in the LSB (bit 0). The reset value is 65408 (0xFF80).

Use this link to go back to the overview table: [ACC_DATA_X_MSB](#).

Register (0x0B) **ACC_DATA_Y_LSB****Description:** Acceleration sample, Y axis LSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	acc_y_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	acc_y_15_0							

- **acc_y_15_0:** (bit offset: 0, bit width: 16, access: read-only) Acceleration Y axis LSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, the saturation flag is encoded here into the LSB (bit 0). The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_DATA_Y_LSB](#).

Register (0x0C) **ACC_DATA_Y_MSB****Description:** Acceleration sample, Y axis MSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	1	1	1	1	1	1	1
Content	acc_y_31_16							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	acc_y_31_16							

- acc_y_31_16: (bit offset: 0, bit width: 16, access: read-only) Acceleration Y axis MSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, please handle correctly the saturation flag in the LSB (bit 0). The reset value is 65408 (0xFF80).

Use this link to go back to the overview table: [ACC_DATA_Y_MSB](#).

Register (0x0D) **ACC_DATA_Z_LSB****Description:** Acceleration sample, Z axis LSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	acc_z_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	acc_z_15_0							

- **acc_z_15_0:** (bit offset: 0, bit width: 16, access: read-only) Acceleration Z axis LSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, the saturation flag is encoded here into the LSB (bit 0). The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_DATA_Z_LSB](#).

Register (0x0E) **ACC_DATA_Z_MSB****Description:** Acceleration sample, Z axis MSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	1	1	1	1	1	1	1
Content	acc_z_31_16							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	acc_z_31_16							

- acc_z_31_16: (bit offset: 0, bit width: 16, access: read-only) Acceleration Z axis MSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, please handle correctly the saturation flag in the LSB (bit 0). The reset value is 65408 (0xFF80).

Use this link to go back to the overview table: [ACC_DATA_Z_MSB](#).

Register (0x0F) **GYR_DATA_X_LSB****Description:** Gyroscope sample, X axis LSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_x_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_x_15_0							

- **gyr_x_15_0:** (bit offset: 0, bit width: 16, access: read-only) Angular rate X axis LSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, the saturation flag is encoded here into the LSB (bit 0). The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_DATA_X_LSB](#).

Register (0x10) **GYR_DATA_X_MSB****Description:** Gyroscope sample, X axis MSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	1	1	1	1	1	1	1
Content	gyr_x_31_16							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	gyr_x_31_16							

- **gyr_x_31_16:** (bit offset: 0, bit width: 16, access: read-only) Angular rate X axis MSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, please handle correctly the saturation flag in the LSB (bit 0). The reset value is 65408 (0xFF80).

Use this link to go back to the overview table: [GYR_DATA_X_MSB](#).

Register (0x11) **GYR_DATA_Y_LSB****Description:** Gyroscope sample, Y axis LSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_y_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_y_15_0							

- **gyr_y_15_0:** (bit offset: 0, bit width: 16, access: read-only) Angular rate Y axis LSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, the saturation flag is encoded here into the LSB (bit 0). The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_DATA_Y_LSB](#).

Register (0x12) **GYR_DATA_Y_MSB****Description:** Gyroscope sample, Y axis MSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	1	1	1	1	1	1	1
Content	gyr_y_31_16							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	gyr_y_31_16							

- **gyr_y_31_16:** (bit offset: 0, bit width: 16, access: read-only) Angular rate Y axis MSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, please handle correctly the saturation flag in the LSB (bit 0). The reset value is 65408 (0xFF80).

Use this link to go back to the overview table: [GYR_DATA_Y_MSB](#).

Register (0x13) **GYR_DATA_Z_LSB****Description:** Gyroscope sample, Z axis LSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_z_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_z_15_0							

- **gyr_z_15_0:** (bit offset: 0, bit width: 16, access: read-only) Angular rate Z axis LSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, the saturation flag is encoded here into the LSB (bit 0). The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_DATA_Z_LSB](#).

Register (0x14) **GYR_DATA_Z_MSB****Description:** Gyroscope sample, Z axis MSB

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	1	1	1	1	1	1	1
Content	gyr_z_31_16							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	gyr_z_31_16							

- **gyr_z_31_16:** (bit offset: 0, bit width: 16, access: read-only) Angular rate Z axis MSB. The data is signed 24 Bit with sign extension to 32 Bit, thus ranging from 0xFF80_0001 to 0x007F_FFFF. If no valid data is available, the reset value of MSB and LSB is read. In case saturation flags are enabled and wide representation is used, please handle correctly the saturation flag in the LSB (bit 0). The reset value is 65408 (0xFF80).

Use this link to go back to the overview table: [GYR_DATA_Z_MSB](#).

Register (0x15) **TEMP_DATA****Description:** Temperature read-out register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	temperature							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	temperature							

- temperature: (bit offset: 0, bit width: 16, access: read-only) Temperature sensor sample. $T (^{\circ}\text{C}) := \text{temp}/256 + 23$. If no valid data is available, 0x8000 is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [TEMP_DATA](#).

Register (0x16) **SENSORTIME_DATA_LSB****Description:** Sensor time, least significant word (15:0)

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	sensortime_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	sensortime_15_0							

- **sensortime_15_0:** (bit offset: 0, bit width: 16, access: read-only) Sensor time data lsb. The reset value is 0 (0x0).

Use this link to go back to the overview table: [SENSORTIME_DATA_LSB](#).

Register (0x17) **SENSORTIME_DATA_MSB****Description:** Sensor time, most significant word (23:16)

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	sensortime_23_16							

- reserved: do not interpret.
- sensortime_23_16: (bit offset: 0, bit width: 8, access: read-only) Sensor time data msb. The reset value is 0 (0x0).

Use this link to go back to the overview table: [SENSORTIME_DATA_MSB](#).

Register (0x18) INT_STATUS_INT1

Description: INT1 Status Register. This register is clear-on-read or clear-on-write configurable.

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	cmd_exe...	reserved	vad_int1	activit...	www_- wgd...	tap_det...	gen_int...	sd_scwm...

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	lp_wup_...	fifo_fu...	fifo_wm...	reserved	drdy_te...	reserved	drdy_gy...	drdy_ac...

- reserved: do not interpret; in case of write, provide the current value.
- drdy_acc_int1: (bit offset: 0, bit width: 1, access: read-write) Accelerometer data ready interrupt status
- drdy_gyr_int1: (bit offset: 1, bit width: 1, access: read-write) Gyroscope data ready interrupt status
- drdy_temp_int1: (bit offset: 3, bit width: 1, access: read-write) Temperature data ready/drive_st (selectable through select register from INT_CONF register) interrupt status
- fifo_wm_int1: (bit offset: 5, bit width: 1, access: read-write) FIFO watermark interrupt status
- fifo_full_int1: (bit offset: 6, bit width: 1, access: read-write) FIFO full interrupt status
- lp_wup_int1: (bit offset: 7, bit width: 1, access: read-write) Low power wake up interrupt status
- sd_scwm_sigmo_int1: (bit offset: 8, bit width: 1, access: read-write) Multiplexed interrupt status for step detector, step counter watermark and significant motion
- gen_int_int1: (bit offset: 9, bit width: 1, access: read-write) Generic interrupt instance (1, 2, 3 and 4) interrupt status
- tap_det_int1: (bit offset: 10, bit width: 1, access: read-write) Tap detector interrupt status
- www_wgd_int1: (bit offset: 11, bit width: 1, access: read-write) Wrist wear wakeup and wrist gesture detection interrupt status
- activity_change_int1: (bit offset: 12, bit width: 1, access: read-write) activity change interrupt status
- vad_int1: (bit offset: 13, bit width: 1, access: read-write) Voice activity detection interrupt status
- cmd_exe_int1: (bit offset: 15, bit width: 1, access: read-write) Command execution status

Use this link to go back to the overview table: [INT_STATUS_INT1](#).

Register (0x19) INT_STATUS_INT2

Description: INT2 Status Register. This register is clear-on-read or clear-on-write configurable.

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	cmd_exe...	reserved	vad_int2	activit...	www_- wgd...	tap_det...	gen_int...	sd_scwm...

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	lp_wup_...	fifo_fu...	fifo_wm...	reserved	drdy_te...	reserved	drdy_gy...	drdy_ac...

- reserved: do not interpret; in case of write, provide the current value.
- drdy_acc_int2: (bit offset: 0, bit width: 1, access: read-write) Accelerometer data ready interrupt status
- drdy_gyr_int2: (bit offset: 1, bit width: 1, access: read-write) Gyroscope data ready interrupt status
- drdy_temp_int2: (bit offset: 3, bit width: 1, access: read-write) Temperature data ready/drive_st (selectable through select register from INT_CONF register) interrupt status
- fifo_wm_int2: (bit offset: 5, bit width: 1, access: read-write) FIFO watermark interrupt status
- fifo_full_int2: (bit offset: 6, bit width: 1, access: read-write) FIFO full interrupt status
- lp_wup_int2: (bit offset: 7, bit width: 1, access: read-write) Low power wake up interrupt status
- sd_scwm_sigmo_int2: (bit offset: 8, bit width: 1, access: read-write) Multiplexed interrupt status for step detector, step counter watermark and significant motion
- gen_int_int2: (bit offset: 9, bit width: 1, access: read-write) Generic interrupt instance (1, 2, 3 and 4) interrupt status
- tap_det_int2: (bit offset: 10, bit width: 1, access: read-write) Tap detector interrupt status
- www_wgd_int2: (bit offset: 11, bit width: 1, access: read-write) Wrist wear wakeup and wrist gesture detection interrupt status
- activity_change_int2: (bit offset: 12, bit width: 1, access: read-write) activity change interrupt status
- vad_int2: (bit offset: 13, bit width: 1, access: read-write) Voice activity detection interrupt status
- cmd_exe_int2: (bit offset: 15, bit width: 1, access: read-write) Command execution status

Use this link to go back to the overview table: [INT_STATUS_INT2](#).

Register (0x1A) INT_STATUS_IBI

Description: I3C IBI Status Register. This register is clear-on-read or clear-on-write configurable.

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	cmd_exe...	reserved	vad_ibi	activit...	www_- wgd...	tap_det...	gen_int...	sd_scwm...

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	lp_wup_ibi	fifo_fu...	fifo_wm...	reserved	drdy_te...	reserved	drdy_gy...	drdy_ac...

- reserved: do not interpret; in case of write, provide the current value.
- drdy_acc_ibi: (bit offset: 0, bit width: 1, access: read-write) Accelerometer data ready interrupt status
- drdy_gyr_ibi: (bit offset: 1, bit width: 1, access: read-write) Gyroscope data ready interrupt status
- drdy_temp_ibi: (bit offset: 3, bit width: 1, access: read-write) Temperature data ready/drive_st (selectable through select register from INT_CONF register) interrupt status
- fifo_wm_ibi: (bit offset: 5, bit width: 1, access: read-write) FIFO watermark interrupt status
- fifo_full_ibi: (bit offset: 6, bit width: 1, access: read-write) FIFO full interrupt status
- lp_wup_ibi: (bit offset: 7, bit width: 1, access: read-write) Low power wake up interrupt status
- sd_scwm_sigmo_ibi: (bit offset: 8, bit width: 1, access: read-write) Multiplexed interrupt status for step detector, step counter watermark and significant motion
- gen_int_ibi: (bit offset: 9, bit width: 1, access: read-write) Generic interrupt instance (1, 2, 3 and 4) interrupt status
- tap_det_ibi: (bit offset: 10, bit width: 1, access: read-write) Tap detector interrupt status
- www_wgd_ibi: (bit offset: 11, bit width: 1, access: read-write) Wrist wear wakeup and wrist gesture detection interrupt status
- activity_change_ibi: (bit offset: 12, bit width: 1, access: read-write) activity change interrupt status
- vad_ibi: (bit offset: 13, bit width: 1, access: read-write) Voice activity detection interrupt status
- cmd_exe_ibi: (bit offset: 15, bit width: 1, access: read-write) Command execution status

Use this link to go back to the overview table: [INT_STATUS_IBI](#).

Register (0x1B) **FEATURE_STATUS_0****Description:** Feature status information register 0

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						status_...	status_...

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	status_...	status_...	status_...	status_...	status_...	status_...	status_...	status_...

- reserved: do not interpret.
- status_step_detect: (bit offset: 0, bit width: 1, access: read-only) Status of step detection
- status_sc_watermark: (bit offset: 1, bit width: 1, access: read-only) Status of step counter watermark event
- status_sig_motion: (bit offset: 2, bit width: 1, access: read-only) Status of significant motion event
- status_any_motion: (bit offset: 3, bit width: 1, access: read-only) Status of any-motion event
- status_no_motion: (bit offset: 4, bit width: 1, access: read-only) Status of no-motion event
- status_low_g: (bit offset: 5, bit width: 1, access: read-only) Status of low-g event
- status_high_g: (bit offset: 6, bit width: 1, access: read-only) Status of high-g event
- status_single_tap: (bit offset: 7, bit width: 1, access: read-only) Status of single tap
- status_double_tap: (bit offset: 8, bit width: 1, access: read-only) Status of double tap
- status_triple_tap: (bit offset: 9, bit width: 1, access: read-only) Status of triple tap

Use this link to go back to the overview table: [FEATURE_STATUS_0](#).

Register (0x1C) **FEATURE_STATUS_1****Description:** Feature status information register 1

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved	detected_activity			wrist_gesture		status_ww_wakeup_...	

- reserved: do not interpret.
- status_ww_wakeup_drop: (bit offset: 0, bit width: 2, access: read-only) Status of Wrist wear wakeup or drop gesture
Following values can be read from the field status_ww_wakeup_drop:

Value	Description
0b00 (0x0) (default)	No Gesture
0b01 (0x1)	Wake-up event
0b10 (0x2)	Drop event

- wrist_gesture: (bit offset: 2, bit width: 2, access: read-only) Detected wrist gesture
Following values can be read from the field wrist_gesture:

Value	Description
0b00 (0x0) (default)	No Gesture
0b01 (0x1)	Jiggle Gesture
0b10 (0x2)	Flick in gesture
0b11 (0x3)	Flick out gesture

- detected_activity: (bit offset: 4, bit width: 3, access: read-only) Detected activity from activity recognizer
Following values can be read from the field detected_activity:

Value	Description
0b000 (0x0) (default)	unknown activity
0b001 (0x1)	still activity detected
0b010 (0x2)	walking activity detected
0b011 (0x3)	running activity detected
0b100 (0x4)	cycling activity detected
0b101 (0x5)	Invehicle detected

Use this link to go back to the overview table: [FEATURE_STATUS_1](#).

Register (0x1D) **FEATURE_STATUS_2****Description:** Feature status information register 2

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	step_count_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	step_count_15_0							

- **step_count_15_0:** (bit offset: 0, bit width: 16, access: read-only) Lower 16-bits of the step count value The reset value is 0 (0x0).

Use this link to go back to the overview table: [FEATURE_STATUS_2](#).

Register (0x1E) **FEATURE_STATUS_3****Description:** Feature status information register 3

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			step_count_20_16				

- reserved: do not interpret.
- step_count_20_16: (bit offset: 0, bit width: 5, access: read-only) Step count value bits 17 to 21 The reset value is 0 (0x0).

Use this link to go back to the overview table: [FEATURE_STATUS_3](#).

Register (0x1F) **FEATURE_IO_0****Description:** Feature engine I/O register 0

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	wrng_ac...	wrng_ac...	cmd_status	cmd_response				

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	cmd_han...	cmd_response_feature					feat_eng_state	

- **feat_eng_state:** (bit offset: 0, bit width: 2, access: read-only) Current operating state of the feature engine. When feature engine is abruptly disabled via FEAT_ENG_GLOB_CTRL, previous operating state will be retained. Following values can be read from the field feat_eng_state:

Value	Description
0b00 (0x0) (default)	feature engine is disabled and no feature processing can be performed on feature engine
0b01 (0x1)	User feature processing mode where feature such as Generic interrupt, tap detector, I3C sync are supported
0b10 (0x2)	Mode in which the self-test or self-calibration of the sensor is executed. Features which are supported in SELF_TEST_CALIB_MODE are ACC_SELF_TEST, GYR_SELF_TEST, ACC_OFFS_EST, GYR_OFFS_EST

- **cmd_response_feature:** (bit offset: 2, bit width: 5, access: read-only) Feature / functionality being executed or last executed by the feature engine with command trigger. Following values can be read from the field cmd_response_feature:

Value	Description
0x0 (default)	No explicit selection
0x2	Self test of accelerometer response
0x3	Self test of gyroscope sense response
0x6	Offset error estimation of gyroscope response
0x8	Offset error estimation of accelerometer response
0x9	Axis remapping response

- **cmd_handler:** (bit offset: 7, bit width: 1, access: read-only) Status indicator on command handling. When a command is received and accepted for processing, the status shall be set to BUSY Status shall be set to READY on completion of the command processing (Outcome can be success / failure) Following values can be read from the field cmd_handler:

Value	Description
0b0 (0x0) (default)	No command processing ongoing, ready to accept command
0b1 (0x1)	Command processing is in-progress, new command will be ignored

- **cmd_response:** (bit offset: 8, bit width: 5, access: read-only) Upon completion of the command processing, host shall

be notified about the outcome of the command processing. Feature processing can complete SUCCESS or FAILURE with ERROR.

Following values can be read from the field `cmd_response`:

Value	Description
0x0 (default)	Reset / Default state - no valid response available yet
0x1	Success with no additional info
0x2	Offset estimation is completed successfully, saturation of results detected
0x11	Sensor boot / start-up error
0x12	Precondition error in starting the feature
0x13	Motion detected during feature processing
0x15	Error in sensor configuration from user interface
0x16	Invalid
0x17	Sanity check failed during feature processing
0x1C	Self-test failed
0x1F	General Error

- `cmd_status`: (bit offset: 13, bit width: 1, access: read-only) When a command is triggered by host, host shall be notified about the status of command acceptance. Command is ignored when a previously received command processing is still on-going.

Following values can be read from the field `cmd_status`:

Value	Description
0b0 (0x0) (default)	Command is accepted for processing
0b1 (0x1)	command ignored due to on-going processing

- `wrng_acc_odr`: (bit offset: 14, bit width: 1, access: read-only) Accelerometer ODR compatibility status with features

Following values can be read from the field `wrng_acc_odr`:

Value	Description
0b0 (0x0) (default)	Accelerometer ODR is compatible with feature requirements
0b1 (0x1)	Accelerometer ODR is incompatible with feature requirements

- `wrng_acc_range`: (bit offset: 15, bit width: 1, access: read-only) Accelerometer range compatibility status with features

Following values can be read from the field `wrng_acc_range`:

Value	Description
0b0 (0x0) (default)	Accelerometer range is compatible with feature requirements
0b1 (0x1)	Accelerometer range is incompatible with feature requirements, Insufficient range selected for sensor core

Use this link to go back to the overview table: [FEATURE_IO_0](#).

Register (0x20) **FEATURE_IO_1**

Description: Feature engine I/O register 1 (requires feature_io_sync to be written to 0b1 before written value can be read-back).

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	dis_fea...	cond_usr2alt_switch				cond_alt2usr_switch		

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	cond_al...	cmd_feature_select					reserved	

- reserved: do not interpret; in case of write, provide the reset value.
- cmd_feature_select: (bit offset: 2, bit width: 5, access: read-write) Feature / functionality to be executed by the feature engine with command trigger.
Following values can be set to or read from the field cmd_feature_select:

Value	Description
0x0 (default)	No explicit selection
0x2	Self test of accelerometer
0x3	Self test of gyroscope sense
0x6	Offset error estimation of gyroscope
0x8	Offset error estimation of accelerometer
0x9	Axis remapping

- cond_alt2usr_switch: (bit offset: 7, bit width: 4, access: read-write) Feature selection for transition switch from alt config to user config
Following values can be set to or read from the field cond_alt2usr_switch:

Value	Description
0b0000 (0x0) (default)	Auto-config switch is disabled
0b0001 (0x1)	Step detection
0b0010 (0x2)	Step counter watermark interrupt
0b0011 (0x3)	Significant motion event
0b0100 (0x4)	generic interrupt any-motion
0b0101 (0x5)	generic interrupt no-motion
0b0110 (0x6)	generic interrupt low-g
0b0111 (0x7)	generic interrupt high-g
0b1000 (0x8)	single tap
0b1001 (0x9)	double tap
0b1010 (0xA)	triple tap
0b1011 (0xB)	Wrist-wear-wakeup event
0b1100 (0xC)	Wrist gesture detection event
0b1101 (0xD)	Activity change event from activity recognizer

0b1110 (0xE)	Voice activity detection event
0b1111 (0xF)	low power wakeup

- **cond_usr2alt_switch:** (bit offset: 11, bit width: 4, access: read-write) Feature selection for transition switch from user config to alt config

Following values can be set to or read from the field `cond_usr2alt_switch`:

Value	Description
0b0000 (0x0) (default)	Auto-config switch is disabled
0b0001 (0x1)	Step detection
0b0010 (0x2)	Step counter watermark interrupt
0b0011 (0x3)	Significant motion event
0b0100 (0x4)	generic interrupt any-motion
0b0101 (0x5)	generic interrupt no-motion
0b0110 (0x6)	generic interrupt low-g
0b0111 (0x7)	generic interrupt high-g
0b1000 (0x8)	single tap
0b1001 (0x9)	double tap
0b1010 (0xA)	triple tap
0b1011 (0xB)	Wrist-wear-wakeup event
0b1100 (0xC)	Wrist gesture detection event
0b1101 (0xD)	Activity change event from activity recognizer
0b1110 (0xE)	Voice activity detection event
0b1111 (0xF)	low power wakeup

- **dis_feat_eng_fifo_on_switch:** (bit offset: 15, bit width: 1, access: read-write) Disable feature engine and FIFO after switch to mode with Low Power Wake Up exit condition

Use this link to go back to the overview table: [FEATURE_IO_1](#).

Register (0x21) **FEATURE_IO_2**

Description: Feature configuration register (requires feature_io_sync to be written to 0b1 before written value can be read-back).

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		en_vad	en_acti...	en_wg_d...	en_ww_w...	en_trip...	en_doub...

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	en_sing...	en_gen_...	en_gen_...	en_gen_...	en_gen_...	en_sig_...	en_step...	en_step...

- reserved: do not interpret; in case of write, provide the reset value.
- en_step_detect: (bit offset: 0, bit width: 1, access: read-write) Enable / disable the step detection
- en_step_count: (bit offset: 1, bit width: 1, access: read-write) Enable / disable the step counting
- en_sig_motion: (bit offset: 2, bit width: 1, access: read-write) Enable / disable significant motion feature
- en_gen_int_anymo: (bit offset: 3, bit width: 1, access: read-write) Enable / disable the generic interrupt any-motion
- en_gen_int_nomo: (bit offset: 4, bit width: 1, access: read-write) Enable / disable the generic interrupt no-motion
- en_gen_int_lowg: (bit offset: 5, bit width: 1, access: read-write) Enable / disable the generic interrupt low-g
- en_gen_int_highg: (bit offset: 6, bit width: 1, access: read-write) Enable / disable the generic interrupt high-g
- en_single_tap: (bit offset: 7, bit width: 1, access: read-write) Enable / disable the single-tap detection by tap detector
- en_double_tap: (bit offset: 8, bit width: 1, access: read-write) Enable / disable the double-tap detection by tap detector
- en_triple_tap: (bit offset: 9, bit width: 1, access: read-write) Enable / disable the triple-tap detection by tap detector
- en_ww_wakeup: (bit offset: 10, bit width: 1, access: read-write) Enable / disable the wrist wear wakeup gesture
- en_wg_detector: (bit offset: 11, bit width: 1, access: read-write) Enable / disable the wrist gesture detector
- en_activity_recognizer: (bit offset: 12, bit width: 1, access: read-write) Enable / disable the activity recognizer
- en_vad: (bit offset: 13, bit width: 1, access: read-write) Enable / disable voice activity detector

Use this link to go back to the overview table: [FEATURE_IO_2](#).

Register (0x22) **FEAT_ENG_SYNC****Description:** Feature engine I/O sync register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							feature...

- reserved: do not interpret; in case of write, provide the current value.
- feature_io_sync: (bit offset: 0, bit width: 1, access: read-write) Write 1 to this bit to apply modifications in FEATURE_IO_x registers. Reads as 1 if changes to FEATURE_IO_x are not yet applied.

Use this link to go back to the overview table: [FEAT_ENG_SYNC](#).

Register (0x23) **FIFO_FILL_LVL****Description:** FIFO fill state in words

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				fifo_fill_lvl			

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	fifo_fill_lvl							

- reserved: do not interpret.
- fifo_fill_lvl: (bit offset: 0, bit width: 12, access: read-only) Current fill level of FIFO buffer. An empty FIFO corresponds to 0x000. The word counter may be reset by reading out all frames from the FIFO buffer or when the FIFO is reset through fifo_flush. The word counter is updated each time a complete frame was read or written. The reset value is 0 (0x0).

Use this link to go back to the overview table: [FIFO_FILL_LVL](#).

Register (0x24) **FIFO_DATA****Description:** FIFO data output register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	fifo_data							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	fifo_data							

- **fifo_data:** (bit offset: 0, bit width: 16, access: read-only) FIFO read data (16 bits). Data format depends on the setting of register FIFO_CONF. The FIFO data are organized in frames. The new data flag is preserved. Read burst access must be used, the address will not increment when the read burst reads at the address of FIFO_DATA. When a frame is only partially read out it is retransmitted including the header at the next readout. When the FIFO is inactive or read empty, 0x8000 is read out as the empty identifier. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [FIFO_DATA](#).

Register (0x25) **FILTER_CONF**

Description: Configuration for filters of accelerometer and gyroscope datapath. Respective accelerometer or gyroscope settings of this register will be applied (if alternate configuration is not active) after write access to ACC_CONF or GYR_CONF.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	reserved				gyr_sat...	reserved	gyr_filter_type	

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	reserved				acc_sat...	reserved	acc_filter_type	

- reserved: do not interpret; in case of write, provide the reset value.
- acc_filter_type: (bit offset: 0, bit width: 2, access: read-write) IIR filter order select
Following values can be set to or read from the field acc_filter_type:

Value	Description
0b00 (0x0)	IIR filter is bypassed
0b01 (0x1)	1st order IIR filter with -20dB roll-off
0b10 (0x2) (default)	2nd order IIR filter with -40dB roll-off
0b11 (0x3)	3rd order IIR filter with -60dB roll-off

- acc_sat_flag_en: (bit offset: 3, bit width: 1, access: read-write) Enables saturation flag capture for accel
- gyr_filter_type: (bit offset: 8, bit width: 2, access: read-write) IIR filter order select
Following values can be set to or read from the field gyr_filter_type:

Value	Description
0b00 (0x0)	IIR filter is bypassed
0b01 (0x1)	1st order IIR filter with -20dB roll-off
0b10 (0x2) (default)	2nd order IIR filter with -40dB roll-off
0b11 (0x3)	3rd order IIR filter with -60dB roll-off

- gyr_sat_flag_en: (bit offset: 11, bit width: 1, access: read-write) Enables saturation flag capture for gyroscope

Use this link to go back to the overview table: [FILTER_CONF](#).

Register (0x26) **ACC_CONF**

Description: Accelerometer configuration register (OTP backed) Sets the output data rate, bandwidth, range and power mode of the accelerometer

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_mode			acc_avg_num			acc_bw	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	1	0	0	0
Content	acc_bw	acc_range			acc_odr			

- **acc_odr:** (bit offset: 0, bit width: 4, access: read-write) Sample rate (ODR) in Hz
Following values can be set to or read from the field acc_odr:

Value	Description
0b0001 (0x1)	ODR = 0.78125Hz
0b0010 (0x2)	ODR = 1.5625Hz
0b0011 (0x3)	ODR = 3.125Hz
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7)	ODR = 50Hz
0b1000 (0x8) (default)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz
0b1011 (0xB)	ODR = 800Hz
0b1100 (0xC)	ODR = 1.6kHz
0b1101 (0xD)	ODR = 3.2kHz
0b1110 (0xE)	ODR = 6.4kHz

- **acc_range:** (bit offset: 4, bit width: 3, access: read-write) Full scale resolution
Following values can be set to or read from the field acc_range:

Value	Description
0b000 (0x0)	+/-2g, available only if legacy_range_conf is set: 61.04μg/LSB
0b001 (0x1)	+/-4g, available only if legacy_range_conf is set: 122.07μg/LSB
0b010 (0x2) (default)	+/-8g, 954ng/LSB (if legacy_range_conf is set: 244.14μg/LSB)
0b011 (0x3)	+/-16g, available only if legacy_range_conf is set: 488.28μg/LSB
0b100 (0x4)	+/-32g, 7.63μg/LSB (if legacy_range_conf is set: 1.953mg/LSB)

- **acc_bw:** (bit offset: 7, bit width: 3, access: read-write) Configure the -3dB cut-off frequency for the accelerometer
Following values can be set to or read from the field acc_bw:

Value	Description
0b000 (0x0) (default)	BW = acc_odr/2 but max 800Hz
0b001 (0x1)	BW = 25Hz
0b010 (0x2)	BW = 50Hz
0b011 (0x3)	BW = 100Hz
0b100 (0x4)	BW = 200Hz
0b101 (0x5)	BW = 400Hz
0b110 (0x6)	BW = 800Hz

- **acc_avg_num:** (bit offset: 10, bit width: 3, access: read-write) Numbers of samples to be averaged
Following values can be set to or read from the field acc_avg_num:

Value	Description
0b000 (0x0) (default)	No averaging; pass sample without filtering
0b001 (0x1)	Averaging of 2 samples
0b010 (0x2)	Averaging of 4 samples
0b011 (0x3)	Averaging of 8 samples
0b100 (0x4)	Averaging of 16 samples
0b101 (0x5)	Averaging of 32 samples
0b110 (0x6)	Averaging of 64 samples

- **acc_mode:** (bit offset: 13, bit width: 3, access: read-write) Operation modes for the accelerometer
Following values can be set to or read from the field acc_mode:

Value	Description
0b000 (0x0) (default)	Disables the accelerometer
0b010 (0x2)	Ultra low power: Enables the accelerometer with sensing operated in duty-cycling and reduced power
0b011 (0x3)	Low power: Enables the accelerometer with sensing operated in duty-cycling
0b100 (0x4)	Normal: Enables the accelerometer in continuous operation state with reduced current
0b111 (0x7)	High performance: Enables the accelerometer in high performance continuous operation state

Use this link to go back to the overview table: [ACC_CONF](#).

Register (0x27) **GYR_CONF**

Description: Gyroscope configuration register (OTP backed) Sets the output data rate, bandwidth, range and the power mode of the Gyroscope in the sensor

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_mode			gyr_avg_num			gyr_bw	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1	1	0	0	0
Content	gyr_bw	gyr_range			gyr_odr			

- **gyr_odr:** (bit offset: 0, bit width: 4, access: read-write) Sample rate (ODR) in Hz
Following values can be set to or read from the field gyr_odr:

Value	Description
0b0001 (0x1)	ODR = 0.78125Hz
0b0010 (0x2)	ODR = 1.5625Hz
0b0011 (0x3)	ODR = 3.125Hz
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7)	ODR = 50Hz
0b1000 (0x8) (default)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz
0b1011 (0xB)	ODR = 800Hz
0b1100 (0xC)	ODR = 1.6kHz
0b1101 (0xD)	ODR = 3.2kHz
0b1110 (0xE)	ODR = 6.4kHz

- **gyr_range:** (bit offset: 4, bit width: 3, access: read-write) Full scale resolution
Following values can be set to or read from the field gyr_range:

Value	Description
0b000 (0x0)	+/-125°/s, available only if legacy_range_conf is set: 3.81mDPS/LSB
0b001 (0x1)	+/-250°/s, available only if legacy_range_conf is set: 7.63mDPS/LSB
0b010 (0x2)	+/-500°/s, available only if legacy_range_conf is set: 15.26mDPS/LSB
0b011 (0x3)	+/-1000°/s, available only if legacy_range_conf is set: 30.52mDPS/LSB
0b100 (0x4)	+/-2000°/s, available only if legacy_range_conf is set: 61.04mDPS/LSB
0b101 (0x5) (default)	+/-4000°/s, 476.8μDPS/LSB (if legacy_range_conf is set: 122.07mDPS/LSB)

- **gyr_bw:** (bit offset: 7, bit width: 3, access: read-write) Configure the -3dB cut-off frequency for the gyroscope
Following values can be set to or read from the field gyr_bw:

Value	Description
0b000 (0x0) (default)	BW = gyr_odr/2 but max 800Hz
0b001 (0x1)	BW = 25Hz
0b010 (0x2)	BW = 50Hz
0b011 (0x3)	BW = 100Hz
0b100 (0x4)	BW = 200Hz
0b101 (0x5)	BW = 400Hz
0b110 (0x6)	BW = 800Hz

- **gyr_avg_num:** (bit offset: 10, bit width: 3, access: read-write) Numbers of samples to be averaged
Following values can be set to or read from the field **gyr_avg_num**:

Value	Description
0b000 (0x0) (default)	No averaging; pass sample without filtering
0b001 (0x1)	Averaging of 2 samples
0b010 (0x2)	Averaging of 4 samples
0b011 (0x3)	Averaging of 8 samples
0b100 (0x4)	Averaging of 16 samples
0b101 (0x5)	Averaging of 32 samples
0b110 (0x6)	Averaging of 64 samples

- **gyr_mode:** (bit offset: 13, bit width: 3, access: read-write) Operation modes for the gyroscope
Following values can be set to or read from the field **gyr_mode**:

Value	Description
0b000 (0x0) (default)	Disables the gyroscope
0b001 (0x1)	Drive-only: Disables the gyroscope but keep the gyroscope drive enabled
0b011 (0x3)	Low power: Enables the gyroscope with sensing operated in duty-cycling (operation below 5°C not recommended)
0b100 (0x4)	Normal: Enables the gyroscope in continuous operation state with reduced current
0b111 (0x7)	High performance: Enables the gyroscope in high performance continuous operation state

Use this link to go back to the overview table: [GYR_CONF](#).

Register (0x29) **ALT_FILTER_CONF**

Description: Alternative configuration for filters of accelerometer and gyroscope datapath. Respective accelerometer or gyroscope settings of this register will be applied (if alternative configuration is active) after write access to ALT_ACC_CONF or ALT_GYR_CONF.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	reserved						alt_gyr_filter_type	

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	reserved						alt_acc_filter_type	

- reserved: do not interpret; in case of write, provide the reset value.
- alt_acc_filter_type: (bit offset: 0, bit width: 2, access: read-write) IIR filter order select
Following values can be set to or read from the field alt_acc_filter_type:

Value	Description
0b00 (0x0)	IIR filter is bypassed
0b01 (0x1)	1st order IIR filter with -20dB roll-off
0b10 (0x2) (default)	2nd order IIR filter with -40dB roll-off
0b11 (0x3)	3rd order IIR filter with -60dB roll-off

- alt_gyr_filter_type: (bit offset: 8, bit width: 2, access: read-write) IIR filter order select
Following values can be set to or read from the field alt_gyr_filter_type:

Value	Description
0b00 (0x0)	IIR filter bypass
0b01 (0x1)	1st order IIR filter with -20dB roll-off
0b10 (0x2) (default)	2nd order IIR filter with -40dB roll-off
0b11 (0x3)	3rd order IIR filter with -60dB roll-off

Use this link to go back to the overview table: [ALT_FILTER_CONF](#).

Register (0x2A) **ALT_ACC_CONF****Description:** Alternative configuration for output data rate, bandwidth, range and power state of the accelerometer

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	alt_acc_mode			alt_acc_avg_num			alt_acc_bw	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	1	0	0	0
Content	alt_acc_bw	alt_acc_range			alt_acc_odr			

- alt_acc_odr: (bit offset: 0, bit width: 4, access: read-write) Sample rate (ODR) in Hz
Following values can be set to or read from the field alt_acc_odr:

Value	Description
0b0001 (0x1)	ODR = 0.78125Hz
0b0010 (0x2)	ODR = 1.5625Hz
0b0011 (0x3)	ODR = 3.125Hz
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7)	ODR = 50Hz
0b1000 (0x8) (default)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz
0b1011 (0xB)	ODR = 800Hz
0b1100 (0xC)	ODR = 1.6kHz
0b1101 (0xD)	ODR = 3.2kHz
0b1110 (0xE)	ODR = 6.4kHz

- alt_acc_range: (bit offset: 4, bit width: 3, access: read-write) Full scale resolution
Following values can be set to or read from the field alt_acc_range:

Value	Description
0b000 (0x0)	+/-2g, available only if legacy_range_conf is set: 61.04μg/LSB
0b001 (0x1)	+/-4g, available only if legacy_range_conf is set: 122.07μg/LSB
0b010 (0x2) (default)	+/-8g, 954ng/LSB (if legacy_range_conf is set: 244.14μg/LSB)
0b011 (0x3)	+/-16g, available only if legacy_range_conf is set: 488.28μg/LSB
0b100 (0x4)	+/-32g, 7.63μg/LSB (if legacy_range_conf is set: 1.953mg/LSB)

- alt_acc_bw: (bit offset: 7, bit width: 3, access: read-write) Configure the -3dB cut-off frequency for the accelerometer
Following values can be set to or read from the field alt_acc_bw:

Value	Description
-------	-------------

0b000 (0x0) (default)	BW = acc_odr/2 but max 800Hz
0b001 (0x1)	BW = 25Hz
0b010 (0x2)	BW = 50Hz
0b011 (0x3)	BW = 100Hz
0b100 (0x4)	BW = 200Hz
0b101 (0x5)	BW = 400Hz
0b110 (0x6)	BW = 800Hz

- alt_acc_avg_num: (bit offset: 10, bit width: 3, access: read-write) Numbers of samples to be averaged
Following values can be set to or read from the field alt_acc_avg_num:

Value	Description
0b000 (0x0) (default)	No averaging; pass sample without filtering
0b001 (0x1)	Averaging of 2 samples
0b010 (0x2)	Averaging of 4 samples
0b011 (0x3)	Averaging of 8 samples
0b100 (0x4)	Averaging of 16 samples
0b101 (0x5)	Averaging of 32 samples
0b110 (0x6)	Averaging of 64 samples

- alt_acc_mode: (bit offset: 13, bit width: 3, access: read-write) Operation modes for the accelerometer
Following values can be set to or read from the field alt_acc_mode:

Value	Description
0b000 (0x0) (default)	Disables the accelerometer
0b010 (0x2)	Ultra low power: Enables the accelerometer with sensing operated in duty-cycling and reduced power
0b011 (0x3)	Low power: Enables the accelerometer with sensing operated in duty-cycling
0b100 (0x4)	Normal: Enables the accelerometer in continuous operation state with reduced current
0b111 (0x7)	High performance: Enables the accelerometer in high performance continuous operation state

Use this link to go back to the overview table: [ALT_ACC_CONF](#).

Register (0x2B) **ALT_GYR_CONF****Description:** Alternative configuration for output data rate, bandwidth, range and power state of the gyroscope

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	alt_gyr_mode			alt_gyr_avg_num			alt_gyr_bw	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1	1	0	0	0
Content	alt_gyr_bw	alt_gyr_range			alt_gyr_odr			

- alt_gyr_odr: (bit offset: 0, bit width: 4, access: read-write) Sample rate (ODR) in Hz
Following values can be set to or read from the field alt_gyr_odr:

Value	Description
0b0001 (0x1)	ODR = 0.78125Hz
0b0010 (0x2)	ODR = 1.5625Hz
0b0011 (0x3)	ODR = 3.125Hz
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7)	ODR = 50Hz
0b1000 (0x8) (default)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz
0b1011 (0xB)	ODR = 800Hz
0b1100 (0xC)	ODR = 1.6kHz
0b1101 (0xD)	ODR = 3.2kHz
0b1110 (0xE)	ODR = 6.4kHz

- alt_gyr_range: (bit offset: 4, bit width: 3, access: read-write) Full scale resolution
Following values can be set to or read from the field alt_gyr_range:

Value	Description
0b000 (0x0)	+/-125°/s, available only if legacy_range_conf is set: 3.81mDPS/LSB
0b001 (0x1)	+/-250°/s, available only if legacy_range_conf is set: 7.63mDPS/LSB
0b010 (0x2)	+/-500°/s, available only if legacy_range_conf is set: 15.26mDPS/LSB
0b011 (0x3)	+/-1000°/s, available only if legacy_range_conf is set: 30.52mDPS/LSB
0b100 (0x4)	+/-2000°/s, available only if legacy_range_conf is set: 61.04mDPS/LSB
0b101 (0x5) (default)	+/-4000°/s, 476.8μDPS/LSB (if legacy_range_conf is set: 122.07mDPS/LSB)

- alt_gyr_bw: (bit offset: 7, bit width: 3, access: read-write) Configure the -3dB cut-off frequency for the gyroscope
Following values can be set to or read from the field alt_gyr_bw:

Value	Description
0b000 (0x0) (default)	BW = gyr_odr/2 but max 800Hz
0b001 (0x1)	BW = 25Hz
0b010 (0x2)	BW = 50Hz
0b011 (0x3)	BW = 100Hz
0b100 (0x4)	BW = 200Hz
0b101 (0x5)	BW = 400Hz
0b110 (0x6)	BW = 800Hz

- **alt_gyr_avg_num:** (bit offset: 10, bit width: 3, access: read-write) Numbers of samples to be averaged
Following values can be set to or read from the field alt_gyr_avg_num:

Value	Description
0b000 (0x0) (default)	No averaging; pass sample without filtering
0b001 (0x1)	Averaging of 2 samples
0b010 (0x2)	Averaging of 4 samples
0b011 (0x3)	Averaging of 8 samples
0b100 (0x4)	Averaging of 16 samples
0b101 (0x5)	Averaging of 32 samples
0b110 (0x6)	Averaging of 64 samples

- **alt_gyr_mode:** (bit offset: 13, bit width: 3, access: read-write) Operation modes for the gyroscope
Following values can be set to or read from the field alt_gyr_mode:

Value	Description
0b000 (0x0) (default)	Disables the gyroscope
0b001 (0x1)	Drive-only: Disables the gyroscope but keep the gyroscope drive enabled
0b011 (0x3)	Low power: Enables the gyroscope with sensing operated in duty-cycling (operation below 5°C not recommended)
0b100 (0x4)	Normal: Enables the gyroscope in continuous operation state with reduced current
0b111 (0x7)	High performance: Enables the gyroscope in high performance continuous operation state

Use this link to go back to the overview table: [ALT_GYR_CONF](#).

Register (0x2C) **ALT_CONF****Description:** Alternative configuration for the device

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R	R	R	R	R	R	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	alt_rst...	reserved						alt_gyr_en

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							alt_acc_en

- reserved: do not interpret; in case of write, provide the reset value.
- alt_acc_en: (bit offset: 0, bit width: 1, access: read-write) Enables switching possibility to an alternate configuration for the accelerometer.
- alt_gyr_en: (bit offset: 8, bit width: 1, access: read-write) Enables switching possibility to an alternate configuration for the gyroscope.
- alt_rst_conf_write_en: (bit offset: 15, bit width: 1, access: read-write) If enabled, any write to ACC_CONF or GYR_CONF will instantly switch back to associated user configuration

Use this link to go back to the overview table: [ALT_CONF](#).

Register (0x2D) ALT_STATUS

Description: Status of alternate configuration Reports the active configuration for the accelerometer and gyroscope

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	1	0	0	1	0	0
Content	reserved							alt_gyr...

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	1	0	0	1	0	0
Content	reserved							alt_acc...

- reserved: do not interpret.
- alt_acc_active: (bit offset: 0, bit width: 1, access: read-only) Accel is using ALT_ACC_CONF if set; ACC_CONF otherwise
- alt_gyr_active: (bit offset: 8, bit width: 1, access: read-only) Gyro is using ALT_GYR_CONF if set; GYR_CONF otherwise

Use this link to go back to the overview table: [ALT_STATUS](#).

Register (0x2E) **SELFTEST_STATUS****Description:** Selftest status / results

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				gyr_st_status		reserved	

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						acc_st_status	

- reserved: do not interpret.
- acc_st_status: (bit offset: 0, bit width: 2, access: read-only) Accel self-test status
Following values can be read from the field acc_st_status:

Value	Description
0b00 (0x0) (default)	Selftest has not been started yet
0b01 (0x1)	Selftest is in progress
0b10 (0x2)	Selftest is done and returned: succeeded
0b11 (0x3)	Selftest is done and returned: fail

- gyr_st_status: (bit offset: 10, bit width: 2, access: read-only) Gyro self-test status of sense channels
Following values can be read from the field gyr_st_status:

Value	Description
0b00 (0x0) (default)	Selftest has not been started yet
0b01 (0x1)	Selftest is in progress
0b10 (0x2)	Selftest is done and returned: succeeded
0b11 (0x3)	Selftest is done and returned: fail

Use this link to go back to the overview table: [SELFTEST_STATUS](#).

Register (0x2F) **HIF_CONFIG**

Description: Configuration option for acknowledgement in registers with clearable fields, for example status information

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							cor_config

- reserved: do not interpret; in case of write, provide the reset value.
- cor_config: (bit offset: 0, bit width: 1, access: read-write)
Following values can be set to or read from the field cor_config:

Value	Description
0b0 (0x0) (default)	clear-on-read (CoR) behaviour where all bits of a register are cleared after it has been read
0b1 (0x1)	clear-on-write (CoW) behaviour where a bit of a register is only cleared by an explicit write to 0b1

Use this link to go back to the overview table: [HIF_CONFIG](#).

Register (0x30) **FIFO_WATERMARK****Description:** FIFO watermark level

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					fifo_watermark		

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	fifo_watermark							

- reserved: do not interpret; in case of write, provide the reset value.
- fifo_watermark: (bit offset: 0, bit width: 11, access: read-write) Trigger an interrupt when FIFO contains fifo_watermark words The reset value is 0 (0x0).

Use this link to go back to the overview table: [FIFO_WATERMARK](#).

Register (0x31) **FIFO_CONF****Description:** Configuration of the FIFO data buffer behaviour

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R/W	R/W	R/W	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		fifo_sensor_time		fifo_te...	reserved	fifo_gy...	fifo_ac...

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						fifo_en	fifo_st...

- reserved: do not interpret; in case of write, provide the reset value.
- fifo_stop_on_full: (bit offset: 0, bit width: 1, access: read-write) Configure whether to overwrite oldest samples when the FIFO data buffer is full
Following values can be set to or read from the field fifo_stop_on_full:

Value	Description
0b0 (0x0) (default)	Continue writing to the data buffer by overwriting oldest samples
0b1 (0x1)	Stop writing into the FIFO data buffer when full

- fifo_en: (bit offset: 1, bit width: 1, access: read-write) Main switch to control whether the FIFO is enabled or not.
Following values can be set to or read from the field fifo_en:

Value	Description
0b0 (0x0) (default)	FIFO is disabled. No data is written into the FIFO memory.
0b1 (0x1)	FIFO is enabled. Data may be written into the FIFO memory.

- fifo_acc_en: (bit offset: 8, bit width: 1, access: read-write) Include 3D acceleration samples from the accelerometer in the FIFO data buffer frames.
Following values can be set to or read from the field fifo_acc_en:

Value	Description
0b0 (0x0) (default)	Accelerometer data not included.
0b1 (0x1)	Accelerometer data is included.

- fifo_gyr_en: (bit offset: 9, bit width: 1, access: read-write) Include 3D angular rate samples from the gyroscope in the FIFO data buffer frames.
Following values can be set to or read from the field fifo_gyr_en:

Value	Description
0b0 (0x0) (default)	Gyroscope data not included.
0b1 (0x1)	Gyroscope data is included.

- fifo_temp_en: (bit offset: 11, bit width: 1, access: read-write) Include temperature sensor data in the FIFO data buffer frames.

Following values can be set to or read from the field `fifo_temp_en`:

Value	Description
0b0 (0x0) (default)	Temperature data not included.
0b1 (0x1)	Temperature data is included.

- `fifo_sensor_time`: (bit offset: 12, bit width: 2, access: read-write) FIFO sensor time configuration

Following values can be set to or read from the field `fifo_sensor_time`:

Value	Description
0b00 (0x0) (default)	No sensor time is recoded in the FIFO data buffer.
0b01 (0x1)	Sensor time is only provided as dedicated frame after FIFO becomes empty during a read burst.
0b10 (0x2)	Current sensor time is included in each FIFO data buffer frame.

Use this link to go back to the overview table: [FIFO_CONF](#).

Register (0x32) **FIFO_CTRL****Description:** Control of the FIFO data buffer

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							fifo_flush

- reserved: do not interpret; in case of write, provide the reset value.
- fifo_flush: (bit offset: 0, bit width: 1, access: write-only) Writing 0b1 clears the FIFO data buffer.

Use this link to go back to the overview table: [FIFO_CTRL](#).

Register (0x33) **IO_INT_CTRL****Description:** Configures the electrical behavior of the interrupt pins

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					int2_ou...	int2_od	int2_lvl

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					int1_ou...	int1_od	int1_lvl

- reserved: do not interpret; in case of write, provide the reset value.
- int1_lvl: (bit offset: 0, bit width: 1, access: read-write) Configure level of INT1 pin
Following values can be set to or read from the field int1_lvl:

Value	Description
0b0 (0x0) (default)	active low
0b1 (0x1)	active high

- int1_od: (bit offset: 1, bit width: 1, access: read-write) Configure behavior of INT1 pin
Following values can be set to or read from the field int1_od:

Value	Description
0b0 (0x0) (default)	push-pull
0b1 (0x1)	open drain

- int1_output_en: (bit offset: 2, bit width: 1, access: read-write) Output enable for INT1 pin
- int2_lvl: (bit offset: 8, bit width: 1, access: read-write) Configure level of INT2 pin
Following values can be set to or read from the field int2_lvl:

Value	Description
0b0 (0x0) (default)	active low
0b1 (0x1)	active high

- int2_od: (bit offset: 9, bit width: 1, access: read-write) Configure behavior of INT2 pin
Following values can be set to or read from the field int2_od:

Value	Description
0b0 (0x0) (default)	push-pull
0b1 (0x1)	open drain

- int2_output_en: (bit offset: 10, bit width: 1, access: read-write) Output enable for INT2 pin

Use this link to go back to the overview table: [IO_INT_CTRL](#).

Register (0x34) **INT_CONF****Description:** Configuration register for INT1 and INT2.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						int2_mode	

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						int1_mode	

- reserved: do not interpret; in case of write, provide the reset value.
- int1_mode: (bit offset: 0, bit width: 2, access: read-write) Configure interrupt output mode for pin INT1
Following values can be set to or read from the field int1_mode:

Value	Description
0b00 (0x0) (default)	Output disabled.
0b01 (0x1)	Latched interrupts mode.
0b10 (0x2)	Pulsed interrupt mode with short pulses.
0b11 (0x3)	Pulsed interrupt mode with long pulses.

- int2_mode: (bit offset: 8, bit width: 2, access: read-write) Configure interrupt output mode for pin INT2
Following values can be set to or read from the field int2_mode:

Value	Description
0b00 (0x0) (default)	Output disabled.
0b01 (0x1)	Latched interrupts mode.
0b10 (0x2)	Pulsed interrupt mode with short pulses.
0b11 (0x3)	Pulsed interrupt mode with long pulses.

Use this link to go back to the overview table: [INT_CONF](#).

Register (0x35) INT_MAP_HW

Description: Interrupt Mapping Register.

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	lp_wup_int_map		fifo_full_int_map		fifo_wm_int_map		reserved	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	temp_drdy_int_map		reserved		gyr_drdy_int_map		acc_drdy_int_map	

- reserved: do not interpret; in case of write, provide the reset value.
- acc_drdy_int_map: (bit offset: 0, bit width: 2, access: read-write) Accelerometer data ready interrupt mapping
Following values can be set to or read from the field acc_drdy_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- gyr_drdy_int_map: (bit offset: 2, bit width: 2, access: read-write) Gyroscope data ready interrupt mapping
Following values can be set to or read from the field gyr_drdy_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- temp_drdy_int_map: (bit offset: 6, bit width: 2, access: read-write) Temperature data ready interrupt mapping
Following values can be set to or read from the field temp_drdy_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- fifo_wm_int_map: (bit offset: 10, bit width: 2, access: read-write) FIFO watermark interrupt mapping
Following values can be set to or read from the field fifo_wm_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)

0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- **fifo_full_int_map:** (bit offset: 12, bit width: 2, access: read-write) FIFO full interrupt mapping
Following values can be set to or read from the field `fifo_full_int_map`:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- **lp_wup_int_map:** (bit offset: 14, bit width: 2, access: read-write) Low power wake up interrupt mapping
Following values can be set to or read from the field `lp_wup_int_map`:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

Use this link to go back to the overview table: [INT_MAP_HW](#).

Register (0x36) INT_MAP_FEAT_ENG

Description: Interrupt Mapping Register for outputs provided by the feature engine ('feat_eng').

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	cmd_exe_map		reserved		vad_map		act_change_map	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	www_wgd_int_map		tap_int_map		gen_int_map		sd_scwm_sigmo_map	

- reserved: do not interpret; in case of write, provide the reset value.
- sd_scwm_sigmo_map: (bit offset: 0, bit width: 2, access: read-write) Multiplexed interrupt mapping for step detector, step counter watermark and significant motion
Following values can be set to or read from the field sd_scwm_sigmo_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- gen_int_map: (bit offset: 2, bit width: 2, access: read-write) Generic interrupt mapping
Following values can be set to or read from the field gen_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- tap_int_map: (bit offset: 4, bit width: 2, access: read-write) Tap interrupt mapping
Following values can be set to or read from the field tap_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- www_wgd_int_map: (bit offset: 6, bit width: 2, access: read-write) wrist wear wakeup and/or wrist gesture detector interrupt mapping
Following values can be set to or read from the field www_wgd_int_map:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- **act_change_map**: (bit offset: 8, bit width: 2, access: read-write) activity change interrupt mapping
Following values can be set to or read from the field **act_change_map**:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- **vad_map**: (bit offset: 10, bit width: 2, access: read-write) Voice activity detection interrupt mapping
Following values can be set to or read from the field **vad_map**:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

- **cmd_exe_map**: (bit offset: 14, bit width: 2, access: read-write) Command execution interrupt mapping
Following values can be set to or read from the field **cmd_exe_map**:

Value	Description
0b00 (0x0) (default)	Interrupt is not mapped to any destination (disabled)
0b01 (0x1)	Interrupt is mapped to INT1 pin
0b10 (0x2)	Interrupt is mapped to INT2 pin
0b11 (0x3)	Interrupt is mapped to I3C in-band interrupts (IBI)

Use this link to go back to the overview table: [INT_MAP_FEAT_ENG](#).

Register (0x37) LPWUP_EN

Description: Low Power Wake Up Enable Register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				lpwup_e...	lpwup_z_ en	lpwup_y_ en	lpwup_x_ en

- reserved: do not interpret; in case of write, provide the reset value.
- lpwup_x_en: (bit offset: 0, bit width: 1, access: read-write) Enable LPWUP on X axis
- lpwup_y_en: (bit offset: 1, bit width: 1, access: read-write) Enable LPWUP on Y axis
- lpwup_z_en: (bit offset: 2, bit width: 1, access: read-write) Enable LPWUP on Z axis
- lpwup_end_en: (bit offset: 3, bit width: 1, access: read-write) Enable LPWUP end detection (on all axes)

Use this link to go back to the overview table: [LPWUP_EN](#).

Register (0x38) **LPWUP_CFG****Description:** Low Power Wake Up Configuration Register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	lpwup_dur			lpwup_ths				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	lpwup_ths							

- **lpwup_ths:** (bit offset: 0, bit width: 13, access: read-write) LPWUP Threshold. $TH = lpwup_ths * 1.95 \text{ mg} + 0.97 \text{ mg}$
The reset value is 0 (0x0).
- **lpwup_dur:** (bit offset: 13, bit width: 3, access: read-write) Sample count (duration) before LPWUP is triggered or its end detected.

Following values can be set to or read from the field lpwup_dur:

Value	Description
0b000 (0x0) (default)	one sample
0b001 (0x1)	two samples
0b010 (0x2)	three samples
0b011 (0x3)	four samples
0b100 (0x4)	five samples
0b101 (0x5)	six samples
0b110 (0x6)	seven samples
0b111 (0x7)	eight samples

Use this link to go back to the overview table: [LPWUP_CFG](#).

Register (0x39) **LPWUP_STATUS****Description:** Low Power Wake Up Status Register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				lpwup_end	lpwup_z	lpwup_y	lpwup_x

- reserved: do not interpret; in case of write, provide the reset value.
- lpwup_x: (bit offset: 0, bit width: 1, access: read-write) LPWUP detected on X axis
- lpwup_y: (bit offset: 1, bit width: 1, access: read-write) LPWUP detected on Y axis
- lpwup_z: (bit offset: 2, bit width: 1, access: read-write) LPWUP detected on Z axis
- lpwup_end: (bit offset: 3, bit width: 1, access: read-write) LPWUP end detected all axes

Use this link to go back to the overview table: [LPWUP_STATUS](#).

Register (0x3A) **FEAT_ENG_GLOB_CTRL****Description:** Global feature engine ('feat_eng') control register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	wake_on...	reserved					feat_eng_mode	

- reserved: do not interpret; in case of write, provide the reset value.
- feat_eng_mode: (bit offset: 0, bit width: 2, access: read-write) feature engine mode. Select the modes of operation. Following values can be set to or read from the field feat_eng_mode:

Value	Description
0b00 (0x0) (default)	Memory is un-powered, feature engine is disabled.
0b01 (0x1)	The feature data port is ready, but the feature engine is disabled.
0b11 (0x3)	The feature data port and feature engine are ready.

- wake_on_trig: (bit offset: 7, bit width: 1, access: read-write) Controls whether the feature engine gets enabled upon a LP-WAKEUP event or not. Following values can be set to or read from the field wake_on_trig:

Value	Description
0b0 (0x0) (default)	The feature engine will not be enabled in case of LP-WAKEUP event
0b1 (0x1)	The feature engine will be enabled in case of LP-WAKEUP event independent of feat_eng_mode setting

Use this link to go back to the overview table: [FEAT_ENG_GLOB_CTRL](#).

Register (0x3B) **FEATURE_DATA_CTRL****Description:** Control data exchange with the feature engine.

Bit	15	14	13	12	11	10	9	8
Read/Write	W	W	R	R	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	data_cmd		reserved		data_addr			

Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	data_addr							

- reserved: do not interpret; in case of write, provide the reset value.
- data_addr: (bit offset: 0, bit width: 12, access: write-only) Start word address for a feature data transaction. This address must be set together with the feature data command. The first feature data read or write is performed on this word address. The address will increment for each subsequent read or write access by 1. Addresses are using word format (16-bit).
Following values can be set to the field data_addr:

Value	Description
0x2	address (0x2) to access register GENERAL_SETTINGS
0x3	address (0x3) to access register FEATURE_ODR_1
0x4	address (0x4) to access register FEATURE_ODR_2
0x7	address (0x7) to access register GEN_INT_ANYMO_1
0x8	address (0x8) to access register GEN_INT_ANYMO_2
0x9	address (0x9) to access register GEN_INT_ANYMO_3
0xA	address (0xa) to access register GEN_INT_ANYMO_4
0xB	address (0xb) to access register GEN_INT_ANYMO_5
0xC	address (0xc) to access register GEN_INT_ANYMO_6
0xD	address (0xd) to access register GEN_INT_ANYMO_7
0xE	address (0xe) to access register GEN_INT_NOMO_1
0xF	address (0xf) to access register GEN_INT_NOMO_2
0x10	address (0x10) to access register GEN_INT_NOMO_3
0x11	address (0x11) to access register GEN_INT_NOMO_4
0x12	address (0x12) to access register GEN_INT_NOMO_5
0x13	address (0x13) to access register GEN_INT_NOMO_6
0x14	address (0x14) to access register GEN_INT_NOMO_7
0x15	address (0x15) to access register GEN_INT_LOWG_1
0x16	address (0x16) to access register GEN_INT_LOWG_2
0x17	address (0x17) to access register GEN_INT_LOWG_3
0x18	address (0x18) to access register GEN_INT_LOWG_4
0x19	address (0x19) to access register GEN_INT_LOWG_5
0x1A	address (0x1a) to access register GEN_INT_LOWG_6
0x1B	address (0x1b) to access register GEN_INT_LOWG_7
0x1C	address (0x1c) to access register GEN_INT_HIGHG_1

0x1D	address (0x1d) to access register GEN_INT_HIGHG_2
0x1E	address (0x1e) to access register GEN_INT_HIGHG_3
0x1F	address (0x1f) to access register GEN_INT_HIGHG_4
0x20	address (0x20) to access register GEN_INT_HIGHG_5
0x21	address (0x21) to access register GEN_INT_HIGHG_6
0x22	address (0x22) to access register GEN_INT_HIGHG_7
0x23	address (0x23) to access register TAP_DETECTOR_1
0x24	address (0x24) to access register TAP_DETECTOR_2
0x25	address (0x25) to access register TAP_DETECTOR_3
0x26	address (0x26) to access register STEP_COUNTER_1
0x27	address (0x27) to access register STEP_COUNTER_2
0x28	address (0x28) to access register STEP_COUNTER_3
0x29	address (0x29) to access register STEP_COUNTER_4
0x2A	address (0x2a) to access register STEP_COUNTER_5
0x2B	address (0x2b) to access register STEP_COUNTER_6
0x2C	address (0x2c) to access register STEP_COUNTER_7
0x2D	address (0x2d) to access register STEP_COUNTER_8
0x2E	address (0x2e) to access register STEP_COUNTER_9
0x2F	address (0x2f) to access register STEP_COUNTER_10
0x30	address (0x30) to access register STEP_COUNTER_11
0x31	address (0x31) to access register STEP_COUNTER_12
0x32	address (0x32) to access register STEP_COUNTER_13
0x33	address (0x33) to access register STEP_COUNTER_14
0x34	address (0x34) to access register STEP_COUNTER_15
0x35	address (0x35) to access register STEP_COUNTER_16
0x36	address (0x36) to access register STEP_COUNTER_17
0x37	address (0x37) to access register STEP_COUNTER_18
0x38	address (0x38) to access register SIGNIFICANT_MOTION_1
0x39	address (0x39) to access register SIGNIFICANT_MOTION_2
0x3A	address (0x3a) to access register SIGNIFICANT_MOTION_3
0x3B	address (0x3b) to access register WRIST_GESTURE_DETECTOR_1
0x3C	address (0x3c) to access register WRIST_GESTURE_DETECTOR_2
0x3D	address (0x3d) to access register WRIST_GESTURE_DETECTOR_3
0x3E	address (0x3e) to access register WRIST_GESTURE_DETECTOR_4
0x3F	address (0x3f) to access register WRIST_GESTURE_DETECTOR_5
0x40	address (0x40) to access register WRIST_GESTURE_DETECTOR_6
0x43	address (0x43) to access register WRIST_GESTURE_DETECTOR_7
0x44	address (0x44) to access register WRIST_GESTURE_DETECTOR_8
0x45	address (0x45) to access register WRIST_WEAR_WAKEUP_1
0x46	address (0x46) to access register WRIST_WEAR_WAKEUP_2
0x47	address (0x47) to access register WRIST_WEAR_WAKEUP_3
0x48	address (0x48) to access register WRIST_WEAR_WAKEUP_4
0x49	address (0x49) to access register WRIST_WEAR_WAKEUP_5

0x4A	address (0x4a) to access register WRIST_WEAR_WAKEUP_6
0x4F	address (0x4f) to access register VAD_1
0x78	address (0x78) to access register ACC_ST
0x7D	address (0x7d) to access register ACC_OFFS_EST_1
0x7E	address (0x7e) to access register GYR_ST_CONF_1
0x7F	address (0x7f) to access register GYR_ST_CONF_2
0x81	address (0x81) to access register GYR_OFFS_EST_1
0x82	address (0x82) to access register GYR_OFFS_EST_2
0x8F	address (0x8f) to access register ST_RESULT
0x90	address (0x90) to access register ACC_OFFS_EST_8G_X
0x91	address (0x91) to access register ACC_OFFS_EST_8G_Y
0x92	address (0x92) to access register ACC_OFFS_EST_8G_Z
0x93	address (0x93) to access register ACC_OFFS_EST_32G_X
0x94	address (0x94) to access register ACC_OFFS_EST_32G_Y
0x95	address (0x95) to access register ACC_OFFS_EST_32G_Z
0x96	address (0x96) to access register GYR_OFFS_EST_X
0x97	address (0x97) to access register GYR_OFFS_EST_Y
0x98	address (0x98) to access register GYR_OFFS_EST_Z
0x9D	address (0x9d) to access register AXIS_MAP

- **data_cmd:** (bit offset: 14, bit width: 2, access: write-only) Command to initialize or terminate a feature data transaction. This control field only shows an effect when feature_data_ready reads '1'.
Following values can be set to the field data_cmd:

Value	Description
0b00 (0x0) (default)	Terminates any active feature data transaction. Strongly recommended after a feature data read or write transaction has been completed.
0b01 (0x1)	Initializes a feature data read transaction. A new feature data read transaction can be initialized without terminating any prior transaction.
0b10 (0x2)	Initializes a feature data write transaction. A new feature data write transaction can be initialized without terminating any prior transaction.

Use this link to go back to the overview table: [FEATURE_DATA_CTRL](#).

Register (0x3C) **FEATURE_DATA_TX**

Description: Write port for the data values to the feature engine. If currently no write transaction is active, writing to this register has no effect.

Bit	15	14	13	12	11	10	9	8
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	data_tx_value							

Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	data_tx_value							

- data_tx_value: (bit offset: 0, bit width: 16, access: write-only) Data to be written to the feature engine The reset value is 0 (0x0).

Use this link to go back to the overview table: [FEATURE_DATA_TX](#).

Register (0x3D) **FEATURE_DATA_RX**

Description: Read port for the data values of the feature engine. If currently no read transaction is active, reading from this register has no effect.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	data_rx_value							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	data_rx_value							

- data_rx_value: (bit offset: 0, bit width: 16, access: read-only) Data to be read from the feature engine The reset value is 0 (0x0).

Use this link to go back to the overview table: [FEATURE_DATA_RX](#).

Register (0x3F) **FEAT_ENG_STATUS****Description:** feature engine ('feat_eng') Status Register.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					data_oo...	feature...	feature...

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	1	0	0	0
Content	reserved			feat_en...	reserved			feat_en...

- reserved: do not interpret.
- feat_eng_halt: (bit offset: 0, bit width: 1, access: read-only) feature engine is enabled but in HALT state, waiting for interrupts.
- feat_eng_rdy: (bit offset: 4, bit width: 1, access: read-only) feature engine has been enabled and the memory is powered.
- feature_data_ready: (bit offset: 8, bit width: 1, access: read-only) Feature data is ready to use. If this bit is 0, feature data access will not work.
- feature_data_active: (bit offset: 9, bit width: 1, access: read-only) Feature data operation and data transactions are ongoing.
- data_oob_err: (bit offset: 10, bit width: 1, access: read-only) Feature data out of bounds error. Cleared on next transaction.

Use this link to go back to the overview table: [FEAT_ENG_STATUS](#).

Register (0x49) **IO_IF_CONF****Description:** Configuration register for the serial interface.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							spi_mode

- reserved: do not interpret; in case of write, provide the reset value.
- spi_mode: (bit offset: 0, bit width: 1, access: read-write) Enable or disable the 3-wire mode for SPI protocol.
Following values can be set to or read from the field spi_mode:

Value	Description
0b0 (0x0) (default)	SPI 4-wire mode
0b1 (0x1)	SPI 3-wire mode

Use this link to go back to the overview table: [IO_IF_CONF](#).

Register (0x4A) **IO_PAD_STRENGTH****Description:** Configuration register for the electrical characteristics of the pads

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			if_proto_force		reserved		

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R/W	R	R	R	R/W	R/W	R/W
Reset Value	0	1	1	0	0	1	0	0
Content	reserved	i2c_boost	reserved			drv_str		

- reserved: do not interpret; in case of write, provide the current value.
- drv_str: (bit offset: 0, bit width: 3, access: read-write) Drive strength control for the output pads of the serial interface: 0:=weakest; 7:=strongest The reset value is 4 (0x4).
- i2c_boost: (bit offset: 6, bit width: 1, access: read-write) Enable or disable the drive strength for SDX when interfacing via I2C. 0b1: enables the default increased drive strength 0b0: does not increase the drive strength
- if_proto_force: (bit offset: 11, bit width: 2, access: read-write) Serial interface protocol force register.
Following values can be set to or read from the field if_proto_force:

Value	Description
0b00 (0x0) (default)	Auto protocol detection for serial interface (I2C/I3C by default with dummy read access to switch to SPI)
0b01 (0x1)	I2C/I3C protocol force, not switching to SPI anymore with CSB toggling. Requires I2C communication and clearing of NVM register to be able to use SPI again.
0b10 (0x2)	SPI protocol force, directly using SPI after power-up. Requires SPI communication and clearing of NVM register to be able to use I2C/I3C again after reboot.
0b11 (0x3)	Not used, Same effect as Auto_detect

Use this link to go back to the overview table: [IO_PAD_STRENGTH](#).

Register (0x4B) **IO_ODR_DEVIATION****Description:** ODR Deviation Trim Register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			odr_deviation				

- reserved: do not interpret.
- odr_deviation: (bit offset: 0, bit width: 5, access: read-only) ODR clock deviation. Part-individual signed value.
 $\text{odr_deviation [\%]} = \text{LSB} * 0.084375 \text{ \% } (-1.35\%..+1.27\%)$ The reset value is 0 (0x0).

Use this link to go back to the overview table: [IO_ODR_DEVIATION](#).

Register (0x54) **LEG_ERR_REG****Description:** Reports sensor error conditions

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		leg_i3c...	leg_i3c...	leg_i3c...	leg_i3c...	leg_i3c...	leg_i3c...

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved	leg_gyr...	leg_acc...	reserved	leg_nvm...	reserved	leg_gyr...	leg_fat...

- reserved: do not interpret; in case of write, provide the current value.
- leg_fatal_err: (bit offset: 0, bit width: 1, access: read-only) Fatal Error, chip is not in operational state (Boot-failure). This flag will be reset only by power-on-reset or softreset.
Following values can be read from the field leg_fatal_err:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- leg_gyr_err: (bit offset: 1, bit width: 1, access: read-only) Gyroscope not operational due to error conditions. This flag will be cleared if gyro is configured to DISABLE by the user.
Following values can be read from the field leg_gyr_err:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- leg_nvm_prog_err: (bit offset: 3, bit width: 1, access: read-only) The command NVM_PROG failed. Bit is reset with next NVM_PROG command.
Following values can be read from the field leg_nvm_prog_err:

Value	Description
0b0 (0x0) (default)	No error during NVM_PROG command execution
0b1 (0x1)	Error during NVM_PROG command execution

- leg_acc_conf_err: (bit offset: 5, bit width: 1, access: read-only) Unsupported accelerometer configuration set by user. This flag will be reset when configuration has been corrected.
Following values can be read from the field leg_acc_conf_err:

Value	Description
0b0 (0x0) (default)	accel sensor configuration okay
0b1 (0x1)	accel sensor configuration invalid

- leg_gyr_conf_err: (bit offset: 6, bit width: 1, access: read-only) Unsupported gyroscope configuration set by user. This flag will be reset when configuration has been corrected.

Following values can be read from the field `leg_gyr_conf_err`:

Value	Description
0b0 (0x0) (default)	gyro sensor configuration okay
0b1 (0x1)	gyro sensor configuration invalid

- `leg_i3c_te0_err`: (bit offset: 8, bit width: 1, access: read-write) Invalid Broadcast Address/W (7'h7E/W) or Dynamic Address/RnW after DA assignment Detect any of the following: 7'h3E / W 7'h5E / W 7'h6E / W 7'h76 / W 7'h7A / W 7'h7C / W 7'h7F / W 7'h7E / R This flag is clear-on-read

Following values can be set to or read from the field `leg_i3c_te0_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `leg_i3c_te1_err`: (bit offset: 9, bit width: 1, access: read-write) CCC Code; Parity Check, using T-Bit; This flag is clear-on-read

Following values can be set to or read from the field `leg_i3c_te1_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `leg_i3c_te2_err`: (bit offset: 10, bit width: 1, access: read-write) Write Data; Parity Check, using T-Bit; This flag is clear-on-read

Following values can be set to or read from the field `leg_i3c_te2_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `leg_i3c_te3_err`: (bit offset: 11, bit width: 1, access: read-write) Assigned Address during Dynamic Address Arbitration; Parity Check, using T-Bit; This flag is clear-on-read

Following values can be set to or read from the field `leg_i3c_te3_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `leg_i3c_te4_err`: (bit offset: 12, bit width: 1, access: read-write) 7'h7E/R missing after Sr during Dynamic Address Arbitration; Detect 7'h7E/R missing after Sr during Dynamic Address Arbitration This flag is clear-on-read

Following values can be set to or read from the field `leg_i3c_te4_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

- `leg_i3c_te5_err`: (bit offset: 13, bit width: 1, access: read-write) Transaction after detecting CCC; Detect illegally formatted CCC; This flag is clear-on-read

Following values can be set to or read from the field `leg_i3c_te5_err`:

Value	Description
0b0 (0x0) (default)	No error
0b1 (0x1)	Error

Use this link to go back to the overview table: [LEG_ERR_REG](#).

Register (0x55) **LEG_STATUS****Description:** Sensor status flags for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R	R	R/W	R/W	R	R	R
Reset Value	1	0	0	0	0	0	1	0
Content	leg_por...	reserved		leg_drd...	leg_drd...	reserved	leg_cmd...	reserved

- reserved: do not interpret; in case of write, provide the current value.
- leg_cmd_rdy: (bit offset: 1, bit width: 1, access: read-only) CMD decoder status for 16bit representation. Following values can be read from the field leg_cmd_rdy:

Value	Description
0b0 (0x0)	Command in progress.
0b1 (0x1) (default)	Command decoder is ready to accept a new command.

- leg_drdy_gyr: (bit offset: 3, bit width: 1, access: read-write) Data ready for Gyroscope. It gets reset, when LEG_STATUS register is read out
- leg_drdy_acc: (bit offset: 4, bit width: 1, access: read-write) Data ready for Accelerometer. It gets reset, when LEG_STATUS register is read out
- leg_por_detected: (bit offset: 7, bit width: 1, access: read-write) Flag is set only after POR. It gets reset, when LEG_STATUS register is read out

Use this link to go back to the overview table: [LEG_STATUS](#).

Register (0x56) **LEG_ACC_DATA_X****Description:** Acceleration sample, X axis for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_acc_x							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_acc_x							

- leg_acc_x: (bit offset: 0, bit width: 16, access: read-only) Accelerometer X axis for 16bit representation. The data is signed 16 Bit, thus ranging from 0x8001 to 0x7FFF. If no valid data is available, the reset value is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_ACC_DATA_X](#).

Register (0x57) **LEG_ACC_DATA_Y****Description:** Acceleration sample, Y axis for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_acc_y							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_acc_y							

- leg_acc_y: (bit offset: 0, bit width: 16, access: read-only) Accelerometer Y axis for 16bit representation. The data is signed 16 Bit, thus ranging from 0x8001 to 0x7FFF. If no valid data is available, the reset value is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_ACC_DATA_Y](#).

Register (0x58) **LEG_ACC_DATA_Z****Description:** Acceleration sample, Z axis for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_acc_z							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_acc_z							

- leg_acc_z: (bit offset: 0, bit width: 16, access: read-only) Accelerometer Z axis for 16bit representation. The data is signed 16 Bit, thus ranging from 0x8001 to 0x7FFF. If no valid data is available, the reset value is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_ACC_DATA_Z](#).

Register (0x59) **LEG_GYR_DATA_X****Description:** Gyroscope sample, X axis for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_gyr_x							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_gyr_x							

- leg_gyr_x: (bit offset: 0, bit width: 16, access: read-only) Gyroscope X axis for 16bit representation. The data is signed 16 Bit, thus ranging from 0x8001 to 0x7FFF. If no valid data is available, the reset value is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_GYR_DATA_X](#).

Register (0x5A) **LEG_GYR_DATA_Y****Description:** Gyroscope sample, Y axis for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_gyr_y							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_gyr_y							

- leg_gyr_y: (bit offset: 0, bit width: 16, access: read-only) Gyroscope Y axis for 16bit representation. The data is signed 16 Bit, thus ranging from 0x8001 to 0x7FFF. If no valid data is available, the reset value is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_GYR_DATA_Y](#).

Register (0x5B) **LEG_GYR_DATA_Z****Description:** Gyroscope sample, Z axis for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_gyr_z							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_gyr_z							

- leg_gyr_z: (bit offset: 0, bit width: 16, access: read-only) Gyroscope Z axis for 16bit representation. The data is signed 16 Bit, thus ranging from 0x8001 to 0x7FFF. If no valid data is available, the reset value is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_GYR_DATA_Z](#).

Register (0x5C) **LEG_TEMP_DATA****Description:** Temperature read-out register for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0
Content	leg_temperature							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_temperature							

- leg_temperature: (bit offset: 0, bit width: 16, access: read-only) Temperature sensor sample for 16bit representation.
 $T (^{\circ}\text{C}) := \text{leg_temperature} / 256 + 23$. If no valid data is available, 0x8000 is read. The reset value is 32768 (0x8000).

Use this link to go back to the overview table: [LEG_TEMP_DATA](#).

Register (0x5D) **LEG_SENSORTIME_DATA_LSB****Description:** Sensor time, least significant word (15:0) for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_sensortime_15_0							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_sensortime_15_0							

- leg_sensortime_15_0: (bit offset: 0, bit width: 16, access: read-only) Sensor time data lsb for 16bit representation. The reset value is 0 (0x0).

Use this link to go back to the overview table: [LEG_SENSORTIME_DATA_LSB](#).

Register (0x5E) **LEG_SENSORTIME_DATA_MSB****Description:** Sensor time, most significant word (23:16) for 16bit representation

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	leg_sensortime_23_16							

- reserved: do not interpret.
- leg_sensortime_23_16: (bit offset: 0, bit width: 8, access: read-only) Sensor time data msb for 16bit representation. The reset value is 0 (0x0).

Use this link to go back to the overview table: [LEG_SENSORTIME_DATA_MSB](#).

Register (0x5F) **SAT_FLAGS****Description:** Saturation flags for each sensor and axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		satf_gyr_z	satf_gyr_y	satf_gyr_x	satf_acc_z	satf_acc_y	satf_acc_x

- reserved: do not interpret.
- satf_acc_x: (bit offset: 0, bit width: 1, access: read-only) Saturation flag for the accelerometer x axis
- satf_acc_y: (bit offset: 1, bit width: 1, access: read-only) Saturation flag for the accelerometer y axis
- satf_acc_z: (bit offset: 2, bit width: 1, access: read-only) Saturation flag for the accelerometer z axis
- satf_gyr_x: (bit offset: 3, bit width: 1, access: read-only) Saturation flag for the gyroscope x axis
- satf_gyr_y: (bit offset: 4, bit width: 1, access: read-only) Saturation flag for the gyroscope y axis
- satf_gyr_z: (bit offset: 5, bit width: 1, access: read-only) Saturation flag for the gyroscope z axis

Use this link to go back to the overview table: [SAT_FLAGS](#).

Register (0x60) **GYR_GAIN_X****Description:** Gyroscope sensitivity re-scale register - Axis X. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_gain_x							

- reserved: do not interpret; in case of write, provide the reset value.
- gyr_gain_x: (bit offset: 0, bit width: 8, access: read-write) Field for the temperature independent gyroscope re-scale, axis X: signed two's complement, 1 LSB = 0.097 % The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_GAIN_X](#).

Register (0x61) **GYR_GAIN_Y**

Description: Gyroscope sensitivity re-scale register - Axis Y. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_gain_y							

- reserved: do not interpret; in case of write, provide the reset value.
- gyr_gain_y: (bit offset: 0, bit width: 8, access: read-write) Field for the temperature independent gyroscope re-scale, axis Y: signed two's complement, 1 LSB = 0.097 % The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_GAIN_Y](#).

Register (0x62) **GYR_GAIN_Z**

Description: Gyroscope sensitivity re-scale register - Axis Z. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_gain_z							

- reserved: do not interpret; in case of write, provide the reset value.
- gyr_gain_z: (bit offset: 0, bit width: 8, access: read-write) Field for the temperature independent gyroscope re-scale, axis Z: signed two's complement, 1 LSB = 0.097 % The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_GAIN_Z](#).

Register (0x64) **ACC_GAIN_X****Description:** Accelerometer sensitivity re-scale register - Axis X

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_gain_x							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_gain_x: (bit offset: 0, bit width: 8, access: read-write) Field for the temperature independent accelerometer re-scale, axis X: signed two's complement, 1 LSB = 0.097 % The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_GAIN_X](#).

Register (0x65) **ACC_GAIN_Y****Description:** Accelerometer sensitivity re-scale register - Axis Y

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_gain_y							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_gain_y: (bit offset: 0, bit width: 8, access: read-write) Field for the temperature independent accelerometer re-scale, axis Y: signed two's complement, 1 LSB = 0.097 % The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_GAIN_Y](#).

Register (0x66) **ACC_GAIN_Z****Description:** Accelerometer sensitivity re-scale register - Axis Z

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_gain_z							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_gain_z: (bit offset: 0, bit width: 8, access: read-write) Field for the temperature independent accelerometer re-scale, axis Z: signed two's complement, 1 LSB = 0.097 % The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_GAIN_Z](#).

Register (0x6A) **GYR_OFFS_X**

Description: Gyroscope offset compensation register - Axis X. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_offs_x							

- reserved: do not interpret; in case of write, provide the reset value.
- gyr_offs_x: (bit offset: 0, bit width: 8, access: read-write) Field for the gyroscope offset compensation, axis X: signed two's complement, 1 LSB = 122 mdps (value can only be read or written while gyr_mode is not off). The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_OFFS_X](#).

Register (0x6B) **GYR_OFFSET_Y**

Description: Gyroscope offset compensation register - Axis Y. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_offset_y							

- reserved: do not interpret; in case of write, provide the reset value.
- gyr_offset_y: (bit offset: 0, bit width: 8, access: read-write) Field for the gyroscope offset compensation, axis Y: signed two's complement, 1 LSB = 122 mdps (value can only be read or written while gyr_mode is not off). The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_OFFSET_Y](#).

Register (0x6C) **GYR_OFFS_Z**

Description: Gyroscope offset compensation register - Axis Z. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gyr_offs_z							

- reserved: do not interpret; in case of write, provide the reset value.
- gyr_offs_z: (bit offset: 0, bit width: 8, access: read-write) Field for the gyroscope offset compensation, axis Z: signed two's complement, 1 LSB = 122 mdps (value can only be read or written while gyr_mode is not off). The reset value is 0 (0x0).

Use this link to go back to the overview table: [GYR_OFFS_Z](#).

Register (0x6E) **ACC_OFFSETS_32G_X**

Description: Accelerometer offset compensation register for 32G range - Axis X. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_offsets_32g_x							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_offsets_32g_x: (bit offset: 0, bit width: 8, access: read-write) Field for the accelerometer offset compensation for 32G range, axis X: signed two's complement, 1 LSB = 7.81 mg The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_OFFSETS_32G_X](#).

Register (0x6F) **ACC_OFFSETS_32G_Y**

Description: Accelerometer offset compensation register for 32G range - Axis Y. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_offs_32g_y							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_offs_32g_y: (bit offset: 0, bit width: 8, access: read-write) Field for the accelerometer offset compensation for 32G range, axis Y: signed two's complement, 1 LSB = 7.81 mg The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_OFFSETS_32G_Y](#).

Register (0x70) **ACC_OFFSETS_32G_Z**

Description: Accelerometer offset compensation register for 32G range - Axis Z. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_offs_32g_z							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_offs_32g_z: (bit offset: 0, bit width: 8, access: read-write) Field for the accelerometer offset compensation for 32G range, axis Y: signed two's complement, 1 LSB = 7.81 mg The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_OFFSETS_32G_Z](#).

Register (0x71) **ACC_OFFSETS_8G_X**

Description: Accelerometer offset compensation register for 8G range - Axis X. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_offsets_8g_x							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_offsets_8g_x: (bit offset: 0, bit width: 8, access: read-write) Field for the accelerometer offset compensation for 8G range, axis X: signed two's complement, 1 LSB = 1.95 mg The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_OFFSETS_8G_X](#).

Register (0x72) **ACC_OFFSETS_8G_Y**

Description: Accelerometer offset compensation register for 8G range - Axis Y. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_offs_8g_y							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_offs_8g_y: (bit offset: 0, bit width: 8, access: read-write) Field for the accelerometer offset compensation for 8G range, axis Y: signed two's complement, 1 LSB = 1.95 mg The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_OFFSETS_8G_Y](#).

Register (0x73) **ACC_OFFSETS_8G_Z**

Description: Accelerometer offset compensation register for 8G range - Axis Z. Persistent value after NVM programming.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_offs_8g_z							

- reserved: do not interpret; in case of write, provide the reset value.
- acc_offs_8g_z: (bit offset: 0, bit width: 8, access: read-write) Field for the accelerometer offset compensation for 8G range, axis Z: signed two's complement, 1 LSB = 1.95 mg The reset value is 0 (0x0).

Use this link to go back to the overview table: [ACC_OFFSETS_8G_Z](#).

Register (0x7B) **LEGACY_CONF****Description:** Configuration register for output data bit-width

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							legacy_...

- reserved: do not interpret; in case of write, provide the reset value.
- legacy_range_conf: (bit offset: 0, bit width: 1, access: read-write) 16bit representation limits output data width of accelerometer and gyroscope to 16bit (regular: 24bit) and enables otherwise unnecessary ranges. This affects also the FIFO frame format!

Following values can be set to or read from the field legacy_range_conf:

Value	Description
0b0 (0x0) (default)	24 bit representation
0b1 (0x1)	16 bit representation (legacy width)

Use this link to go back to the overview table: [LEGACY_CONF](#).

Register (0x7C) **PWR_CONF****Description:** Power mode configuration register

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							adv_pow...

- reserved: do not interpret; in case of write, provide the current value.
- adv_power_save: (bit offset: 0, bit width: 1, access: read-write) Advanced power save If set: allows automatic disabling of all internal clocks if no sensor is enabled.

Use this link to go back to the overview table: [PWR_CONF](#).

Register (0x7E) **CMD****Description:** Command Register

Bit	15	14	13	12	11	10	9	8
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	cmd							

Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	cmd							

- cmd: (bit offset: 0, bit width: 16, access: write-only) Available commands (Note: Register will always return 0x00 as read result):

Following values can be set to the field cmd:

Value	Description
0x100	Trigger the command related features based on FEATURE_IO_1.cmd_feature_select
0xC0DE	Trigger NVM User Prog: Do NVM_ERASE + NVM_PROG but for the user register pairs in NVM
0xDEAF	Triggers a reset, all user configuration settings are overwritten with their default state

Use this link to go back to the overview table: [CMD](#).

7.2 Extended Register Map Description

The extended configuration and input/output of the feature engine has to be done through the feature engine data interface. Data can be read from `FEATURE_DATA_RX` or written through `FEATURE_DATA_TX` from/to an address in the extended register map configured in `FEATURE_DATA_CTRL` by a data exchange transaction. To start such a transaction the read/write direction has to be defined via `FEATURE_DATA_CTRL.data_cmd` and the desired address selected via `FEATURE_DATA_CTRL.data_addr` in a single access to `FEATURE_DATA_CTRL`. Next, all data for this transaction can be continuously read from `FEATURE_DATA_RX` (burst read) or written to `FEATURE_DATA_TX` (burst write), see Fig. 32. As a last step, the transaction has to be terminated by writing 0b0 into `FEATURE_DATA_CTRL.data_cmd`.

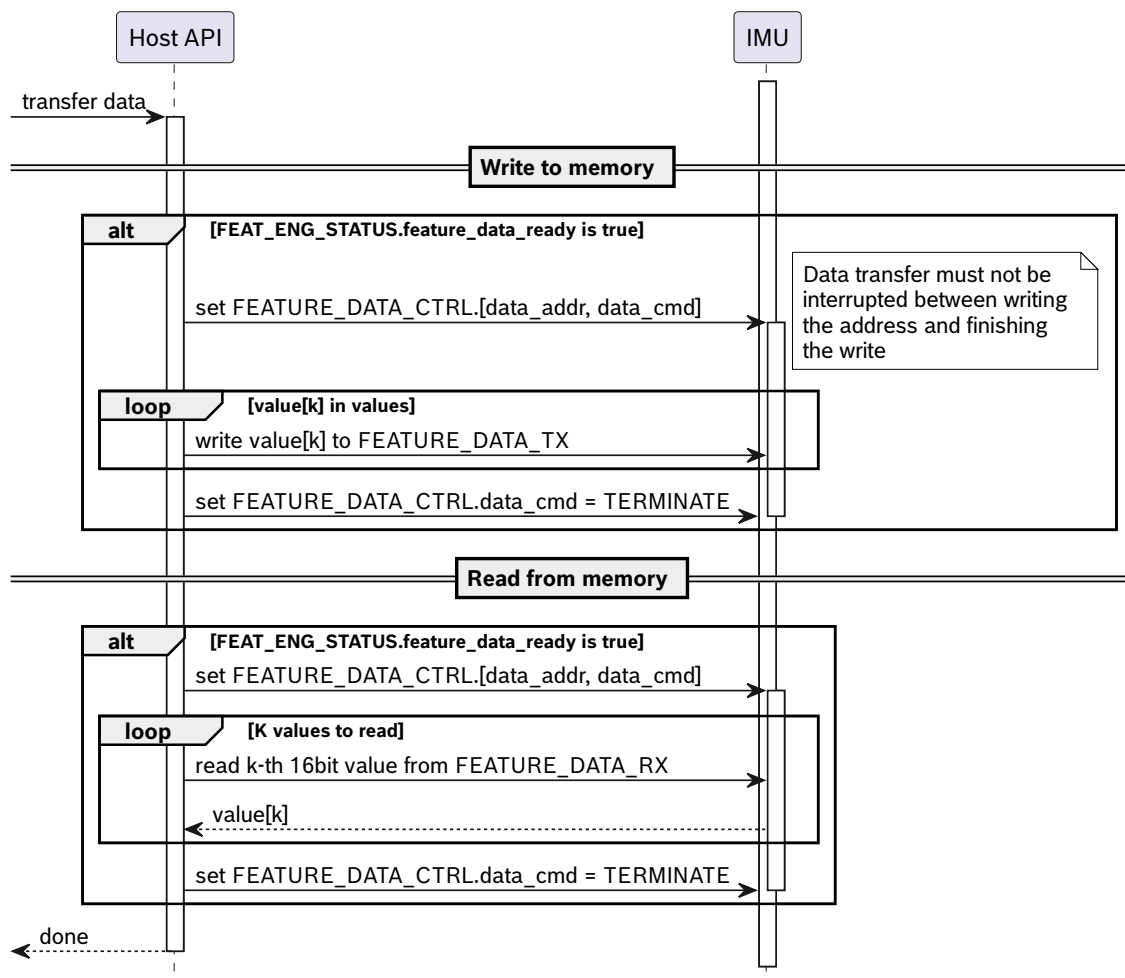


Figure 32: Data transfer to and from the extended register

The status of the data transfer is reported in the register `FEAT_ENG_STATUS`:

- `FEAT_ENG_STATUS.feature_data_ready` is set to 0b1 by the device if data can be read from or written to the feature engine
- `FEAT_ENG_STATUS.data_oob_err` is set to 0b1 by the device if the provided address is outside the specified register address range, see table 7.2.1
- `FEAT_ENG_STATUS.feature_data_active` is set to 0b1 by the device if a transaction via the feature engine data interface is ongoing until it's actively terminated.

The next section 7.2.1 provides an overview of the register file as map and section 7.2.2 explains details for all registers the fields with their purpose.

7.2.1 Extended Register Map

Table 58 provides an overview of the extended register map of the feature engine.

Table 58: Extended Register Map Overview²

Legend			Read-only				Read/Write				Write-only				Reserved				
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
...	-	-	reserved																
0x02	GENERAL_SETTINGS	0x0000	reserved																opt_sw_...
0x03	FEATURE_ODR_1	0x7777	rate_highg				rate_lowg				rate_nomo				rate_anymo				
0x04	FEATURE_ODR_2	0x7777	wgd_sample_rate				www_sample_rate				sigmo_sample_rate				sc_sample_rate				
...	-	-	reserved																
0x07	GEN_INT_ANYMO_1	0xE00F	axis_sel_anymo			comb_se...	slope_thres_anymo												
0x08	GEN_INT_ANYMO_2	0x0C03	reserved			acc_ref_up_anymo		criteri...	hysteresis_anymo										
0x09	GEN_INT_ANYMO_3	0xA00A	wait_time_anymo			duration_anymo													
0x0A	GEN_INT_ANYMO_4	0x0040	reserved			quiet_time_anymo													
0x0B	GEN_INT_ANYMO_5	0x0000	ref_acc_x_anymo																
0x0C	GEN_INT_ANYMO_6	0x0000	ref_acc_y_anymo																
0x0D	GEN_INT_ANYMO_7	0x0800	ref_acc_z_anymo																
0x0E	GEN_INT_NOMO_1	0xF00F	axis_sel_nomo			comb_se...	slope_thres_nomo												
0x0F	GEN_INT_NOMO_2	0x0803	reserved			acc_ref_up_nomo		criteri...	hysteresis_nomo										
0x10	GEN_INT_NOMO_3	0xA00A	wait_time_nomo			duration_nomo													
0x11	GEN_INT_NOMO_4	0x0040	reserved			quiet_time_nomo													
0x12	GEN_INT_NOMO_5	0x0000	ref_acc_x_nomo																
0x13	GEN_INT_NOMO_6	0x0000	ref_acc_y_nomo																
0x14	GEN_INT_NOMO_7	0x0800	ref_acc_z_nomo																
0x15	GEN_INT_LOWG_1	0xF082	axis_sel_lowg			comb_se...	slope_thres_lowg												
0x16	GEN_INT_LOWG_2	0x1008	reserved			acc_ref_up_lowg		criteri...	hysteresis_lowg										
0x17	GEN_INT_LOWG_3	0x4003	wait_time_lowg			duration_lowg													
0x18	GEN_INT_LOWG_4	0x0040	reserved			quiet_time_lowg													
0x19	GEN_INT_LOWG_5	0x0000	ref_acc_x_lowg																
0x1A	GEN_INT_LOWG_6	0x0000	ref_acc_y_lowg																
0x1B	GEN_INT_LOWG_7	0x0000	ref_acc_z_lowg																
0x1C	GEN_INT_HIGHG_1	0xE300	axis_sel_highg			comb_se...	slope_thres_highg												

²Long register and field names are abbreviated with '...'. When hovering over '...' most PDF viewers display the full name.

Table 58: Extended Register Map Overview (continued)

Legend			Read-only				Read/Write				Write-only				Reserved					
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
0x1D	GEN_INT_HIGHG_2	0x1420	reserved			acc_ref_up_highg		criteri...		hysteresis_highg										
0x1E	GEN_INT_HIGHG_3	0xA00A	wait_time_highg			duration_highg														
0x1F	GEN_INT_HIGHG_4	0x0040	reserved			quiet_time_highg														
0x20	GEN_INT_HIGHG_5	0x0000	ref_acc_x_highg																	
0x21	GEN_INT_HIGHG_6	0x0000	ref_acc_y_highg																	
0x22	GEN_INT_HIGHG_7	0x0000	ref_acc_z_highg																	
0x23	TAP_DETECTOR_1	0x0076	reserved								mode		max_peaks_for_tap			wait_fo...		axis_sel		
0x24	TAP_DETECTOR_2	0x402D	max_gesture_dur						tap_peak_thres											
0x25	TAP_DETECTOR_3	0x6864	quiet_time_after_gesture					min_quiet_dur_between_taps					tap_shock_settling_dur				max_dur_between_peaks			
0x26	STEP_COUNTER_1	0x0000	reserved	reset_c...	sc_wm_level															
0x27	STEP_COUNTER_2	0x012D	envelope_up_thres																	
0x28	STEP_COUNTER_3	0xF7A8	envelope_up_decay_coeff																	
0x29	STEP_COUNTER_4	0x013B	envelope_down_thres																	
0x2A	STEP_COUNTER_5	0xF5B6	envelope_down_decay_coeff																	
0x2B	STEP_COUNTER_6	0xF67E	acc_mean_decay_coeff																	
0x2C	STEP_COUNTER_7	0xD99A	step_dur_mean_decay_coeff																	
0x2D	STEP_COUNTER_8	0x6014	reserved	en_half...	step_counter_increment										filter_...		step_buffer_size			
0x2E	STEP_COUNTER_9	0x1927	peak_duration_min_running								peak_duration_min_walking									
0x2F	STEP_COUNTER_10	0xF3C3	activity_detection_thres												activity_detection_factor					
0x30	STEP_COUNTER_11	0xA096	step_duration_window								step_duration_max									
0x31	STEP_COUNTER_12	0x01D7	reserved						mcr_thres						en_mcr_pp		step_dur_thres			en_step...
0x32	STEP_COUNTER_13	0x04C3	config_param_1																	
0x33	STEP_COUNTER_14	0x0985	config_param_2																	
0x34	STEP_COUNTER_15	0x04C3	config_param_3																	
0x35	STEP_COUNTER_16	0xE6EC	config_param_4																	
0x36	STEP_COUNTER_17	0x460B	config_param_5																	
0x37	STEP_COUNTER_18	0x0E0E	config_param_6																	
0x38	SIGNIFICANT_MOTION_1	0x1432	segment_count								segment_size									
0x39	SIGNIFICANT_MOTION_2	0x4426	mcr_min								p2p_min									
0x3A	SIGNIFICANT_MOTION_3	0x4653	mcr_max								p2p_max									
0x3B	WRIST_GESTURE_DET...	0x0640	min_flick_peak_y_threshold																	
0x3C	WRIST_GESTURE_DET...	0x02BC	min_flick_peak_z_threshold																	
0x3D	WRIST_GESTURE_DET...	0xFC00	gravity_bound_x_neg																	

Table 58: Extended Register Map Overview (continued)

Legend			Read-only				Read/Write				Write-only				Reserved					
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
0x3E	WRIST_GESTURE_DET...	0x0784	gravity_bound_x_pos																	
0x3F	WRIST_GESTURE_DET...	0xFC3F	gravity_bound_y_neg																	
0x40	WRIST_GESTURE_DET...	0xF912	gravity_bound_z_neg																	
...	-	-	reserved																	
0x43	WRIST_GESTURE_DET...	0x0010	max_duration_jiggle_peaks																	
0x44	WRIST_GESTURE_DET...	0x0000	reserved															device_...		
0x45	WRIST_WEAR_WAKEUP_1	0xF116	angle_portrait_up								angle_portrait_down									
0x46	WRIST_WEAR_WAKEUP_2	0x8080	angle_landscape_left								angle_landscape_right									
0x47	WRIST_WEAR_WAKEUP_3	0x0621	min_angle_non_focus_pose																	
0x48	WRIST_WEAR_WAKEUP_4	0x06C9	min_angle_focus_pose																	
0x49	WRIST_WEAR_WAKEUP_5	0x0202	min_dur_static								min_dur_in_motion									
0x4A	WRIST_WEAR_WAKEUP_6	0x0000	reserved															enable_...	enable_...	
...	-	-	reserved																	
0x4F	VAD_1	0x14AF	reserved			cls_mode	reserved										en_vad_chnl			
...	-	-	reserved																	
0x78	ACC_ST	0x0099	reserved						sig_int_thres		en_sig_...	samples_to_settle			samples_to_meas					
...	-	-	reserved																	
0x7D	ACC_OFFS_EST_1	0x0893	axis_1g			reserved	apply_corr	reserved	sig_int_thres		en_sig_...	samples_to_settle			samples_to_measure					
0x7E	GYR_ST_CONF_1	0x08A3	reserved						sig_int_thres		en_sig_...	samples_to_settle			samples_to_measure					
0x7F	GYR_ST_CONF_2	0x001A	reserved												motion_detect_thres			en_moti...		
...	-	-	reserved																	
0x81	GYR_OFFS_EST_1	0x0922	reserved				apply_corr	reserved	sig_int_thres		en_sig_...	samples_to_settle			samples_to_measure					
0x82	GYR_OFFS_EST_2	0x001A	reserved												motion_detect_thres			en_moti...		
...	-	-	reserved																	
0x8F	ST_RESULT	0x0000	reserved								gyr_st_ok	acc_st_ok	gyr_dri...	gyr_sen...	gyr_sen...	gyr_sen...	acc_sen...	acc_sen...	acc_sen...	
0x90	ACC_OFFS_EST_8G_X	0x0000	reserved								offs_est_8g_x									
0x91	ACC_OFFS_EST_8G_Y	0x0000	reserved								offs_est_8g_y									
0x92	ACC_OFFS_EST_8G_Z	0x0000	reserved								offs_est_8g_z									
0x93	ACC_OFFS_EST_32G_X	0x0000	reserved								offs_est_32g_x									
0x94	ACC_OFFS_EST_32G_Y	0x0000	reserved								offs_est_32g_y									
0x95	ACC_OFFS_EST_32G_Z	0x0000	reserved								offs_est_32g_z									
0x96	GYR_OFFS_EST_X	0x0000	reserved								offs_est_x									

Table 58: Extended Register Map Overview (continued)

Legend			Read-only				Read/Write				Write-only				Reserved			
Addr	Name	Reset value	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x97	GYR_OFFS_EST_Y	0x0000	reserved								offs_est_y							
0x98	GYR_OFFS_EST_Z	0x0000	reserved								offs_est_z							
...	-	-	reserved															
0x9D	AXIS_MAP	0x0000	reserved										invert_z	invert_y	invert_x	axis_ex		
...	-	-	reserved															

7.2.2 Extended Register Map Details

Register (0x02) **GENERAL_SETTINGS**

Description: Configuration parameters common across all features

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							opt_sw_...

- reserved: do not interpret; in case of write, provide the reset value.
- opt_sw_pwr_save_en: (bit offset: 0, bit width: 1, access: read-write) Enable optimal power saving option in SW, applicable only in LPM/ULPM
Following values can be set to or read from the field opt_sw_pwr_save_en:

Value	Description
0b0 (0x0) (default)	Disable optimal power saving option in SW
0b1 (0x1)	Enable optimal power saving option in SW

Use this link to go back to the overview table: [GENERAL_SETTINGS](#).

Register (0x03) **FEATURE_ODR_1****Description:** Operating sample rates of generic interrupt features

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	1	1	1
Content	rate_highg				rate_lowg			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	1	1	1
Content	rate_nomo				rate_anymo			

- **rate_anymo:** (bit offset: 0, bit width: 4, access: read-write) Operating sample rate of Any-Motion feature
Following values can be set to or read from the field rate_anymo:

Value	Description
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz
0b1000 (0x8)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz

- **rate_nomo:** (bit offset: 4, bit width: 4, access: read-write) Operating sample rate of No-Motion feature
Following values can be set to or read from the field rate_nomo:

Value	Description
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz
0b1000 (0x8)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz

- **rate_lowg:** (bit offset: 8, bit width: 4, access: read-write) Operating sample rate of Low-G feature
Following values can be set to or read from the field rate_lowg:

Value	Description
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz
0b1000 (0x8)	ODR = 100Hz

0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz

- **rate_highg:** (bit offset: 12, bit width: 4, access: read-write) Operating sample rate of High-G feature
Following values can be set to or read from the field **rate_highg**:

Value	Description
0b0100 (0x4)	ODR = 6.25Hz
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz
0b1000 (0x8)	ODR = 100Hz
0b1001 (0x9)	ODR = 200Hz
0b1010 (0xA)	ODR = 400Hz

Use this link to go back to the overview table: [FEATURE_ODR_1](#).

Register (0x04) **FEATURE_ODR_2**

Description: Execution sample rate of step counter, significant motion, wrist wear wakeup and wrist gesture detector

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	1	1	1
Content	wgd_sample_rate				www_sample_rate			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	1	1	1
Content	sigmo_sample_rate				sc_sample_rate			

- **sc_sample_rate:** (bit offset: 0, bit width: 4, access: read-write) Operating sample rate of step counter
Following values can be set to or read from the field **sc_sample_rate**:

Value	Description
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz

- **sigmo_sample_rate:** (bit offset: 4, bit width: 4, access: read-write) Operating sample rate of significant motion
Following values can be set to or read from the field **sigmo_sample_rate**:

Value	Description
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz

- **www_sample_rate:** (bit offset: 8, bit width: 4, access: read-write) Operating sample rate of wrist wear wakeup
Following values can be set to or read from the field **www_sample_rate**:

Value	Description
0b0101 (0x5)	ODR = 12.5Hz
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz

- **wgd_sample_rate:** (bit offset: 12, bit width: 4, access: read-write) Operating sample rate of wrist gesture detector
Following values can be set to or read from the field **wgd_sample_rate**:

Value	Description
0b0110 (0x6)	ODR = 25Hz
0b0111 (0x7) (default)	ODR = 50Hz

Use this link to go back to the overview table: [FEATURE_ODR_2](#).

Register (0x07) **GEN_INT_ANYMO_1**

Description: Configuration of acceleration slope threshold, axis enabling and evaluation condition between axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	0	0	0
Content	axis_sel_anymo			comb_se...	slope_thres_anymo			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	1
Content	slope_thres_anymo							

- **slope_thres_anymo:** (bit offset: 0, bit width: 12, access: read-write) Minimum/maximum slope of acceleration signal for interrupt detection based on selected motion criterion. The reset value is 15 (0xF). The field slope_thres_anymo has the following properties:

Property	Value
Bitwidth	12
Sign	unsigned
Unit	g
Scaling	512.0
Default value	15/512
Range	Min=0.0, Max=7.998046875

- **comb_sel_anymo:** (bit offset: 12, bit width: 1, access: read-write) Logical evaluation condition between enabled axis status
Following values can be set to or read from the field comb_sel_anymo:

Value	Description
0b0 (0x0) (default)	One of the enabled axis should meet the set condition
0b1 (0x1)	All of the enabled axis should meet the set condition

- **axis_sel_anymo:** (bit offset: 13, bit width: 3, access: read-write) Enabling of axis for any-motion detection
Following values can be set to or read from the field axis_sel_anymo:

Value	Description
0b001 (0x1)	Select x-axis for any-motion
0b010 (0x2)	Select y-axis for any-motion
0b011 (0x3)	Select x- and y-axis for any-motion
0b100 (0x4)	Select z-axis for any-motion
0b101 (0x5)	Select x- and z-axis selection for any-motion
0b110 (0x6)	Select y- and z-axis for any-motion
0b111 (0x7) (default)	Select x-, y- and z-axis for any-motion

Use this link to go back to the overview table: [GEN_INT_ANYMO_1](#).

Register (0x08) **GEN_INT_ANYMO_2**

Description: Configuration for hysteresis of acceleration slope, motion criterion selection and reference update mode selection.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	0	0
Content	reserved			acc_ref_up_anymo		criteri...	hysteresis_anymo	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Content	hysteresis_anymo							

- reserved: do not interpret; in case of write, provide the reset value.
- hysteresis_anymo: (bit offset: 0, bit width: 10, access: read-write) Hysteresis for the slope of the acceleration signal. The reset value is 3 (0x3). The field hysteresis_anymo has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512.0
Default value	3/512
Range	Min=0.0, Max=1.998046875

- criterion_sel_anymo: (bit offset: 10, bit width: 1, access: read-write) Selection of motion criterion. Following values can be set to or read from the field criterion_sel_anymo:

Value	Description
0b0 (0x0)	Evaluate the condition for stationary state of the device
0b1 (0x1) (default)	Evaluate the condition for motion state of the device

- acc_ref_up_anymo: (bit offset: 11, bit width: 2, access: read-write) Mode of the acceleration reference update. Following values can be set to or read from the field acc_ref_up_anymo:

Value	Description
0b00 (0x0)	On detection of the event
0b01 (0x1) (default)	On update of acceleration signal
0b10 (0x2)	Manually update by host

Use this link to go back to the overview table: [GEN_INT_ANYMO_2](#).

Register (0x09) **GEN_INT_ANYMO_3**

Description: Configuration of timing related parameters for detection of any-motion events by generic interrupt

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	0	0	0	0
Content	wait_time_anymo			duration_anymo				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	1	0
Content	duration_anymo							

- duration_anymo: (bit offset: 0, bit width: 13, access: read-write) Minimum duration for which the selected criterion is true for interrupt detection. The reset value is 10 (0xA). The field duration_anymo has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.2
Range	Min=0.0, Max=163.82

- wait_time_anymo: (bit offset: 13, bit width: 3, access: read-write) Wait time for clearing the event after condition evaluates false The reset value is 5 (0x5). The field wait_time_anymo has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.1
Range	Min=0.0, Max=0.14

Use this link to go back to the overview table: [GEN_INT_ANYMO_3](#).

Register (0x0A) **GEN_INT_ANYMO_4****Description:** Configuration for quiet time between interrupts

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			quiet_time_anymo				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	quiet_time_anymo							

- reserved: do not interpret; in case of write, provide the reset value.
- quiet_time_anymo: (bit offset: 0, bit width: 13, access: read-write) Quiet time after an interrupt where no additional interrupts are detected The reset value is 64 (0x40). The field quiet_time_anymo has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	1.28
Range	Min=0.0, Max=163.82

Use this link to go back to the overview table: [GEN_INT_ANYMO_4](#).

Register (0x0B) **GEN_INT_ANYMO_5****Description:** Manually set acceleration signal reference for x-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_anymo							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_anymo							

- ref_acc_x_anymo: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for x-axis The reset value is 0 (0x0). The field ref_acc_x_anymo has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_ANYMO_5](#).

Register (0x0C) **GEN_INT_ANYMO_6****Description:** Manually set acceleration signal reference for y-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_anymo							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_anymo							

- ref_acc_y_anymo: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for y-axis The reset value is 0 (0x0). The field ref_acc_y_anymo has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_ANYMO_6](#).

Register (0x0D) **GEN_INT_ANYMO_7****Description:** Manually set acceleration signal reference for z-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	ref_acc_z_anymo							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_z_anymo							

- ref_acc_z_anymo: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for z-axis The reset value is 2048 (0x800). The field ref_acc_z_anymo has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	1.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_ANYMO_7](#).

Register (0x0E) **GEN_INT_NOMO_1**

Description: Configuration of acceleration slope threshold, axis enabling and evaluation condition between axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	0	0	0
Content	axis_sel_nomo			comb_se...	slope_thres_nomo			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	1
Content	slope_thres_nomo							

- **slope_thres_nomo:** (bit offset: 0, bit width: 12, access: read-write) Minimum/maximum slope of acceleration signal for interrupt detection based on selected motion criterion. The reset value is 15 (0xF). The field slope_thres_nomo has the following properties:

Property	Value
Bitwidth	12
Sign	unsigned
Unit	g
Scaling	512.0
Default value	15/512
Range	Min=0.0, Max=7.998046875

- **comb_sel_nomo:** (bit offset: 12, bit width: 1, access: read-write) Logical evaluation condition between enabled axis status

Following values can be set to or read from the field comb_sel_nomo:

Value	Description
0b0 (0x0)	One of the enabled axis should meet the set condition
0b1 (0x1) (default)	All of the enabled axis should meet the set condition

- **axis_sel_nomo:** (bit offset: 13, bit width: 3, access: read-write) Enabling of axis for no-motion detection

Following values can be set to or read from the field axis_sel_nomo:

Value	Description
0b001 (0x1)	Select x-axis for no-motion
0b010 (0x2)	Select y-axis for no-motion
0b011 (0x3)	Select x- and y-axis for no-motion
0b100 (0x4)	Select z-axis for no-motion
0b101 (0x5)	Select x- and z-axis selection for no-motion
0b110 (0x6)	Select y- and z-axis for no-motion
0b111 (0x7) (default)	Select x-, y- and z-axis for no-motion

Use this link to go back to the overview table: [GEN_INT_NOMO_1](#).

Register (0x0F) **GEN_INT_NOMO_2**

Description: Configuration for hysteresis of acceleration slope, motion criterion selection and reference update mode selection.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	reserved			acc_ref_up_nomo		criteri...	hysteresis_nomo	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Content	hysteresis_nomo							

- reserved: do not interpret; in case of write, provide the reset value.
- hysteresis_nomo: (bit offset: 0, bit width: 10, access: read-write) Hysteresis for the slope of the acceleration signal. The reset value is 3 (0x3). The field hysteresis_nomo has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512.0
Default value	3/512
Range	Min=0.0, Max=1.998046875

- criterion_sel_nomo: (bit offset: 10, bit width: 1, access: read-write) Selection of motion criterion. Following values can be set to or read from the field criterion_sel_nomo:

Value	Description
0b0 (0x0) (default)	Evaluate the condition for stationary state of the device
0b1 (0x1)	Evaluate the condition for motion state of the device

- acc_ref_up_nomo: (bit offset: 11, bit width: 2, access: read-write) Mode of the acceleration reference update. Following values can be set to or read from the field acc_ref_up_nomo:

Value	Description
0b00 (0x0)	On detection of the event
0b01 (0x1) (default)	On update of acceleration signal
0b10 (0x2)	Manually update by host

Use this link to go back to the overview table: [GEN_INT_NOMO_2](#).

Register (0x10) **GEN_INT_NOMO_3**

Description: Configuration of timing related parameters for detection of no-motion events by generic interrupt

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	0	0	0	0
Content	wait_time_nomo			duration_nomo				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	1	0
Content	duration_nomo							

- duration_nomo: (bit offset: 0, bit width: 13, access: read-write) Minimum duration for which the selected criterion is true for interrupt detection. The reset value is 10 (0xA). The field duration_nomo has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.2
Range	Min=0.0, Max=163.82

- wait_time_nomo: (bit offset: 13, bit width: 3, access: read-write) Wait time for clearing the event after condition evaluates false The reset value is 5 (0x5). The field wait_time_nomo has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.1
Range	Min=0.0, Max=0.14

Use this link to go back to the overview table: [GEN_INT_NOMO_3](#).

Register (0x11) **GEN_INT_NOMO_4****Description:** Configuration for quiet time between interrupts

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			quiet_time_nomo				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	quiet_time_nomo							

- reserved: do not interpret; in case of write, provide the reset value.
- quiet_time_nomo: (bit offset: 0, bit width: 13, access: read-write) Quiet time after an interrupt where no additional interrupts are detected The reset value is 64 (0x40). The field quiet_time_nomo has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	1.28
Range	Min=0.0, Max=163.82

Use this link to go back to the overview table: [GEN_INT_NOMO_4](#).

Register (0x12) **GEN_INT_NOMO_5**

Description: Manually set acceleration signal reference for x-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_nomo							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_nomo							

- ref_acc_x_nomo: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for x-axis The reset value is 0 (0x0). The field ref_acc_x_nomo has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_NOMO_5](#).

Register (0x13) **GEN_INT_NOMO_6****Description:** Manually set acceleration signal reference for y-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_nomo							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_nomo							

- ref_acc_y_nomo: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for y-axis The reset value is 0 (0x0). The field ref_acc_y_nomo has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_NOMO_6](#).

Register (0x14) **GEN_INT_NOMO_7****Description:** Manually set acceleration signal reference for z-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	ref_acc_z_nomo							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_z_nomo							

- ref_acc_z_nomo: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for z-axis The reset value is 2048 (0x800). The field ref_acc_z_nomo has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	1.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_NOMO_7](#).

Register (0x15) **GEN_INT_LOWG_1**

Description: Configuration of acceleration slope threshold, axis enabling and evaluation condition between axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	0	0	0
Content	axis_sel_lowg			comb_se...	slope_thres_lowg			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	1	0
Content	slope_thres_lowg							

- **slope_thres_lowg:** (bit offset: 0, bit width: 12, access: read-write) Minimum/maximum slope of acceleration signal for interrupt detection based on selected motion criterion. The reset value is 130 (0x82). The field **slope_thres_lowg** has the following properties:

Property	Value
Bitwidth	12
Sign	unsigned
Unit	g
Scaling	512.0
Default value	130/512
Range	Min=0.0, Max=7.998046875

- **comb_sel_lowg:** (bit offset: 12, bit width: 1, access: read-write) Logical evaluation condition between enabled axis status
Following values can be set to or read from the field **comb_sel_lowg**:

Value	Description
0b0 (0x0)	One of the enabled axis should meet the set condition
0b1 (0x1) (default)	All of the enabled axis should meet the set condition

- **axis_sel_lowg:** (bit offset: 13, bit width: 3, access: read-write) Enabling of axis for low-g detection
Following values can be set to or read from the field **axis_sel_lowg**:

Value	Description
0b001 (0x1)	Select x-axis for low-g
0b010 (0x2)	Select y-axis for low-g
0b011 (0x3)	Select x- and y-axis for low-g
0b100 (0x4)	Select z-axis for low-g
0b101 (0x5)	Select x- and z-axis selection for low-g
0b110 (0x6)	Select y- and z-axis for low-g
0b111 (0x7) (default)	Select x-, y- and z-axis for low-g

Use this link to go back to the overview table: [GEN_INT_LOWG_1](#).

Register (0x16) **GEN_INT_LOWG_2**

Description: Configuration for hysteresis of acceleration slope, motion criterion selection and reference update mode selection.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	0	0
Content	reserved			acc_ref_up_lowg		criteri...	hysteresis_lowg	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	hysteresis_lowg							

- reserved: do not interpret; in case of write, provide the reset value.
- hysteresis_lowg: (bit offset: 0, bit width: 10, access: read-write) Hysteresis for the slope of the acceleration signal. The reset value is 8 (0x8). The field hysteresis_lowg has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512.0
Default value	8/512
Range	Min=0.0, Max=1.998046875

- criterion_sel_lowg: (bit offset: 10, bit width: 1, access: read-write) Selection of motion criterion. Following values can be set to or read from the field criterion_sel_lowg:

Value	Description
0b0 (0x0) (default)	Evaluate the condition for stationary state of the device
0b1 (0x1)	Evaluate the condition for motion state of the device

- acc_ref_up_lowg: (bit offset: 11, bit width: 2, access: read-write) Mode of the acceleration reference update. Following values can be set to or read from the field acc_ref_up_lowg:

Value	Description
0b00 (0x0)	On detection of the event
0b01 (0x1)	On update of acceleration signal
0b10 (0x2) (default)	Manually update by host

Use this link to go back to the overview table: [GEN_INT_LOWG_2](#).

Register (0x17) **GEN_INT_LOWG_3**

Description: Configuration of timing related parameters for detection of low-g events by generic interrupt

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	wait_time_lowg			duration_lowg				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Content	duration_lowg							

- duration_lowg: (bit offset: 0, bit width: 13, access: read-write) Minimum duration for which the selected criterion is true for interrupt detection. The reset value is 3 (0x3). The field duration_lowg has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.06
Range	Min=0.0, Max=163.82

- wait_time_lowg: (bit offset: 13, bit width: 3, access: read-write) Wait time for clearing the event after condition evaluates false The reset value is 2 (0x2). The field wait_time_lowg has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.04
Range	Min=0.0, Max=0.14

Use this link to go back to the overview table: [GEN_INT_LOWG_3](#).

Register (0x18) **GEN_INT_LOWG_4****Description:** Configuration for quiet time between interrupts

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			quiet_time_lowg				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	quiet_time_lowg							

- reserved: do not interpret; in case of write, provide the reset value.
- quiet_time_lowg: (bit offset: 0, bit width: 13, access: read-write) Quiet time after an interrupt where no additional interrupts are detected The reset value is 64 (0x40). The field quiet_time_lowg has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	1.28
Range	Min=0.0, Max=163.82

Use this link to go back to the overview table: [GEN_INT_LOWG_4](#).

Register (0x19) **GEN_INT_LOWG_5****Description:** Manually set acceleration signal reference for x-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_lowg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_lowg							

- **ref_acc_x_lowg:** (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for x-axis The reset value is 0 (0x0). The field ref_acc_x_lowg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_LOWG_5](#).

Register (0x1A) **GEN_INT_LOWG_6****Description:** Manually set acceleration signal reference for y-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_lowg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_lowg							

- ref_acc_y_lowg: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for y-axis The reset value is 0 (0x0). The field ref_acc_y_lowg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_LOWG_6](#).

Register (0x1B) **GEN_INT_LOWG_7****Description:** Manually set acceleration signal reference for z-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_z_lowg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_z_lowg							

- ref_acc_z_lowg: (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for z-axis The reset value is 0 (0x0). The field ref_acc_z_lowg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_LOWG_7](#).

Register (0x1C) **GEN_INT_HIGHG_1**

Description: Configuration of acceleration slope threshold, axis enabling and evaluation condition between axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	0	1	1
Content	axis_sel_highg			comb_se...	slope_thres_highg			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	slope_thres_highg							

- **slope_thres_highg:** (bit offset: 0, bit width: 12, access: read-write) Minimum/maximum slope of acceleration signal for interrupt detection based on selected motion criterion. The reset value is 768 (0x300). The field slope_thres_highg has the following properties:

Property	Value
Bitwidth	12
Sign	unsigned
Unit	g
Scaling	512.0
Default value	768/512
Range	Min=0.0, Max=7.998046875

- **comb_sel_highg:** (bit offset: 12, bit width: 1, access: read-write) Logical evaluation condition between enabled axis status

Following values can be set to or read from the field comb_sel_highg:

Value	Description
0b0 (0x0) (default)	One of the enabled axis should meet the set condition
0b1 (0x1)	All of the enabled axis should meet the set condition

- **axis_sel_highg:** (bit offset: 13, bit width: 3, access: read-write) Enabling of axis for high-g detection

Following values can be set to or read from the field axis_sel_highg:

Value	Description
0b001 (0x1)	Select x-axis for high-g
0b010 (0x2)	Select y-axis for high-g
0b011 (0x3)	Select x- and y-axis for high-g
0b100 (0x4)	Select z-axis for high-g
0b101 (0x5)	Select x- and z-axis selection for high-g
0b110 (0x6)	Select y- and z-axis for high-g
0b111 (0x7) (default)	Select x-, y- and z-axis for high-g

Use this link to go back to the overview table: [GEN_INT_HIGHG_1](#).

Register (0x1D) **GEN_INT_HIGHG_2**

Description: Configuration for hysteresis of acceleration slope, motion criterion selection and reference update mode selection.

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	1	0	0
Content	reserved			acc_ref_up_highg		criteri...	hysteresis_highg	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	0	0	0
Content	hysteresis_highg							

- reserved: do not interpret; in case of write, provide the reset value.
- hysteresis_highg: (bit offset: 0, bit width: 10, access: read-write) Hysteresis for the slope of the acceleration signal. The reset value is 32 (0x20). The field hysteresis_highg has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512.0
Default value	32/512
Range	Min=0.0, Max=1.998046875

- criterion_sel_highg: (bit offset: 10, bit width: 1, access: read-write) Selection of motion criterion. Following values can be set to or read from the field criterion_sel_highg:

Value	Description
0b0 (0x0)	Evaluate the condition for stationary state of the device
0b1 (0x1) (default)	Evaluate the condition for motion state of the device

- acc_ref_up_highg: (bit offset: 11, bit width: 2, access: read-write) Mode of the acceleration reference update. Following values can be set to or read from the field acc_ref_up_highg:

Value	Description
0b00 (0x0)	On detection of the event
0b01 (0x1)	On update of acceleration signal
0b10 (0x2) (default)	Manually update by host

Use this link to go back to the overview table: [GEN_INT_HIGHG_2](#).

Register (0x1E) **GEN_INT_HIGHG_3**

Description: Configuration of timing related parameters for detection of high-g events by generic interrupt

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	0	0	0	0
Content	wait_time_highg			duration_highg				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	1	0
Content	duration_highg							

- duration_highg: (bit offset: 0, bit width: 13, access: read-write) Minimum duration for which the selected criterion is true for interrupt detection. The reset value is 10 (0xA). The field duration_highg has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.2
Range	Min=0.0, Max=163.82

- wait_time_highg: (bit offset: 13, bit width: 3, access: read-write) Wait time for clearing the event after condition evaluates false The reset value is 5 (0x5). The field wait_time_highg has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	s
Scaling	50.0
Default value	0.1
Range	Min=0.0, Max=0.14

Use this link to go back to the overview table: [GEN_INT_HIGHG_3](#).

Register (0x1F) **GEN_INT_HIGHG_4****Description:** Configuration for quiet time between interrupts

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved			quiet_time_highg				

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	quiet_time_highg							

- reserved: do not interpret; in case of write, provide the reset value.
- quiet_time_highg: (bit offset: 0, bit width: 13, access: read-write) Quiet time after an interrupt where no additional interrupts are detected The reset value is 64 (0x40). The field quiet_time_highg has the following properties:

Property	Value
Bitwidth	13
Sign	unsigned
Unit	s
Scaling	50.0
Default value	1.28
Range	Min=0.0, Max=163.82

Use this link to go back to the overview table: [GEN_INT_HIGHG_4](#).

Register (0x20) **GEN_INT_HIGHG_5****Description:** Manually set acceleration signal reference for x-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_highg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_x_highg							

- **ref_acc_x_highg:** (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for x-axis The reset value is 0 (0x0). The field ref_acc_x_highg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_HIGHG_5](#).

Register (0x21) **GEN_INT_HIGHG_6****Description:** Manually set acceleration signal reference for y-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_highg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_y_highg							

- **ref_acc_y_highg:** (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for y-axis The reset value is 0 (0x0). The field ref_acc_y_highg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_HIGHG_6](#).

Register (0x22) **GEN_INT_HIGHG_7****Description:** Manually set acceleration signal reference for z-axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_z_highg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	ref_acc_z_highg							

- **ref_acc_z_highg:** (bit offset: 0, bit width: 16, access: read-write) Reference acceleration signal for z-axis The reset value is 0 (0x0). The field ref_acc_z_highg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048.0
Default value	0.0
Range	Min=-16.0, Max=15.99951171875

Use this link to go back to the overview table: [GEN_INT_HIGHG_7](#).

Register (0x23) **TAP_DETECTOR_1****Description:** Selection of the tap detection axis, gesture reporting approach, detection mode

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	1	1	0
Content	mode		max_peaks_for_tap			wait_fo...	axis_sel	

- reserved: do not interpret; in case of write, provide the reset value.
- axis_sel: (bit offset: 0, bit width: 2, access: read-write) Dominant sensing axis of accelerometer along which tap gesture is performed
Following values can be set to or read from the field axis_sel:

Value	Description
0b00 (0x0)	Use x-axis for tap detection
0b01 (0x1)	Use y-axis for tap detection
0b10 (0x2) (default)	Use z-axis for tap detection

- wait_for_timeout: (bit offset: 2, bit width: 1, access: read-write) Perform gesture confirmation with wait time set by max_gesture_dur
Following values can be set to or read from the field wait_for_timeout:

Value	Description
0b0 (0x0)	Report the gesture when detected
0b1 (0x1) (default)	Report the gesture after confirmation

- max_peaks_for_tap: (bit offset: 3, bit width: 3, access: read-write) Maximum number of threshold crossing expected around a tap The reset value is 6 (0x6).
- mode: (bit offset: 6, bit width: 2, access: read-write) Mode for detection of tap gesture. Default value = Normal. In stable position of device, to improve detection accuracy, sensitive mode can be used. Under noisy scenarios, the false detection can be suppressed with Robust mode
Following values can be set to or read from the field mode:

Value	Description
0b00 (0x0)	Sensitive detection mode
0b01 (0x1) (default)	Normal detection mode
0b10 (0x2)	Robust detection mode

Use this link to go back to the overview table: [TAP_DETECTOR_1](#).

Register (0x24) **TAP_DETECTOR_2****Description:** Tap detector setting

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	max_gesture_dur						tap_peak_thres	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	1	1	0	1
Content	tap_peak_thres							

- **tap_peak_thres:** (bit offset: 0, bit width: 10, access: read-write) Minimum threshold for peak resulting from the tap. The reset value is 45 (0x2D). The field tap_peak_thres has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512
Default value	45/512
Range	Min=0.0, Max=1.998046875

- **max_gesture_dur:** (bit offset: 10, bit width: 6, access: read-write) Maximum duration from first tap within the second and/or third tap is expected to happen. The reset value is 16 (0x10). The field max_gesture_dur has the following properties:

Property	Value
Bitwidth	6
Sign	unsigned
Unit	s
Scaling	25
Default value	0.64
Range	Min=0.0, Max=2.52

Use this link to go back to the overview table: [TAP_DETECTOR_2](#).

Register (0x25) **TAP_DETECTOR_3****Description:** Tap detector setting

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	0	1	0	0	0
Content	quiet_time_after_gesture				min_quiet_dur_between_taps			

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	0	0	1	0	0
Content	tap_shock_settling_dur				max_dur_between_peaks			

- **max_dur_between_peaks:** (bit offset: 0, bit width: 4, access: read-write) Maximum duration between positive and negative peaks to tap The reset value is 4 (0x4). The field max_dur_between_peaks has the following properties:

Property	Value
Bitwidth	4
Sign	unsigned
Unit	s
Scaling	200
Default value	0.02
Range	Min=0.0, Max=0.075

- **tap_shock_settling_dur:** (bit offset: 4, bit width: 4, access: read-write) Maximum duration for which tap impact is observed The reset value is 6 (0x6). The field tap_shock_settling_dur has the following properties:

Property	Value
Bitwidth	4
Sign	unsigned
Unit	s
Scaling	200
Default value	0.03
Range	Min=0.0, Max=0.075

- **min_quiet_dur_between_taps:** (bit offset: 8, bit width: 4, access: read-write) Minimum duration between two consecutive tap impact The reset value is 8 (0x8). The field min_quiet_dur_between_taps has the following properties:

Property	Value
Bitwidth	4
Sign	unsigned
Unit	s
Scaling	200
Default value	0.04
Range	Min=0.0, Max=0.075

- **quiet_time_after_gesture:** (bit offset: 12, bit width: 4, access: read-write) Minimum quiet duration between two gestures The reset value is 6 (0x6). The field quiet_time_after_gesture has the following properties:

Property	Value
Bitwidth	4
Sign	unsigned
Unit	s
Scaling	25
Default value	0.24
Range	Min=0.0, Max=0.6

Use this link to go back to the overview table: [TAP_DETECTOR_3](#).

Register (0x26) **STEP_COUNTER_1****Description:** Configuration for step counter watermark interrupt, restart of step counting and filter customization

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved	reset_c...	sc_wm_level					

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	sc_wm_level							

- reserved: do not interpret; in case of write, provide the reset value.
- sc_wm_level: (bit offset: 0, bit width: 14, access: read-write) Selection of step counter level for watermark interrupt. An interrupt will be triggered every time there is step count increment by watermark level from last event. If 0, the interrupt is disabled. The reset value is 0 (0x0).
- reset_counter: (bit offset: 14, bit width: 1, access: read-write) Reset the step count. Auto cleared after reset. Following values can be set to or read from the field reset_counter:

Value	Description
0b0 (0x0) (default)	Do not reset
0b1 (0x1)	Reset step count

Use this link to go back to the overview table: [STEP_COUNTER_1](#).

Register (0x27) **STEP_COUNTER_2****Description:** Threshold for upper peak of acceleration magnitude for step detection

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Content	envelope_up_thres							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	1	1	0	1
Content	envelope_up_thres							

- envelope_up_thres: (bit offset: 0, bit width: 16, access: read-write) Threshold for upper peak of acceleration magnitude for step detection The reset value is 301 (0x12D). The field envelope_up_thres has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	g
Scaling	2048.0
Default value	301/2048
Range	Min=0.0, Max=15.99951171875

Use this link to go back to the overview table: [STEP_COUNTER_2](#).

Register (0x28) **STEP_COUNTER_3****Description:** Adaptive upper peak threshold decay coefficient

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	1	1	1
Content	envelope_up_decay_coeff							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	0	0
Content	envelope_up_decay_coeff							

- envelope_up_decay_coeff: (bit offset: 0, bit width: 16, access: read-write) Adaptive upper peak threshold decay coefficient The reset value is 63400 (0xF7A8). The field envelope_up_decay_coeff has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Scaling	65536.0
Default value	63400/65536
Range	Min=0.0, Max=0.999984741210938

Use this link to go back to the overview table: [STEP_COUNTER_3](#).

Register (0x29) **STEP_COUNTER_4****Description:** Threshold for lower peak of acceleration magnitude for step detection

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Content	envelope_down_thres							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	0	1	1
Content	envelope_down_thres							

- **envelope_down_thres:** (bit offset: 0, bit width: 16, access: read-write) Threshold for lower peak of acceleration magnitude for step detection The reset value is 315 (0x13B). The field **envelope_down_thres** has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	g
Scaling	2048.0
Default value	315/2048
Range	Min=0.0, Max=15.99951171875

Use this link to go back to the overview table: [STEP_COUNTER_4](#).

Register (0x2A) **STEP_COUNTER_5****Description:** Adaptive lower peak threshold decay coefficient

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	1	0	1
Content	envelope_down_decay_coeff							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	1	0	1	1	0
Content	envelope_down_decay_coeff							

- envelope_down_decay_coeff: (bit offset: 0, bit width: 16, access: read-write) Adaptive lower peak threshold decay coefficient The reset value is 62902 (0xF5B6). The field envelope_down_decay_coeff has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Scaling	65536.0
Default value	62902/65536
Range	Min=0.0, Max=0.999984741210938

Use this link to go back to the overview table: [STEP_COUNTER_5](#).

Register (0x2B) **STEP_COUNTER_6****Description:** Exponential smoothing filter coefficient for computing mean of acceleration magnitude

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	1	1	0
Content	acc_mean_decay_coeff							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	1	1	1	0
Content	acc_mean_decay_coeff							

- **acc_mean_decay_coeff:** (bit offset: 0, bit width: 16, access: read-write) Exponential smoothing filter coefficient for computing mean of acceleration magnitude. The reset value is 63102 (0xF67E). The field **acc_mean_decay_coeff** has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Scaling	65536.0
Default value	63102/65536
Range	Min=0.0, Max=0.999984741210938

Use this link to go back to the overview table: [STEP_COUNTER_6](#).

Register (0x2C) **STEP_COUNTER_7****Description:** Exponential smoothing filter coefficient for computing mean duration between steps

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	1	1	0	0	1
Content	step_dur_mean_decay_coeff							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	1	0	1	0
Content	step_dur_mean_decay_coeff							

- **step_dur_mean_decay_coeff:** (bit offset: 0, bit width: 16, access: read-write) Exponential smoothing filter coefficient for computing mean duration between steps The reset value is 55706 (0xD99A). The field **step_dur_mean_decay_coeff** has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Scaling	65536.0
Default value	55706/65536
Range	Min=0.0, Max=0.999984741210938

Use this link to go back to the overview table: [STEP_COUNTER_7](#).

Register (0x2D) **STEP_COUNTER_8****Description:** Configuration of step buffer size, filter cascading and step counter increment factor

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	0	0	0	0	0
Content	reserved	en_half...	step_counter_increment					

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	1	0	0
Content	step_counter_increment			filter_...	step_buffer_size			

- reserved: do not interpret; in case of write, provide the reset value.
- step_buffer_size: (bit offset: 0, bit width: 4, access: read-write) Minimum number of consecutive steps to be detected for updating step count The reset value is 4 (0x4).
- filter_cascade_enabled: (bit offset: 4, bit width: 1, access: read-write) Enable or disable cascading of filters
- step_counter_increment: (bit offset: 5, bit width: 9, access: read-write) Scale factor for the step count to handle overcounting to undercounting The reset value is 256 (0x100). The field step_counter_increment has the following properties:

Property	Value
Bitwidth	9
Scaling	256
Default value	1
Range	Min=0, Max=1.99609375

- en_half_step: (bit offset: 14, bit width: 1, access: read-write) Enable or disable detection of half step

Use this link to go back to the overview table: [STEP_COUNTER_8](#).

Register (0x2E) **STEP_COUNTER_9****Description:** Configuration of minimum duration between two consecutive steps while walking and running

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	0	0	1
Content	peak_duration_min_running							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	1	1	1
Content	peak_duration_min_walking							

- **peak_duration_min_walking:** (bit offset: 0, bit width: 8, access: read-write) Minimum duration between two consecutive steps while walking The reset value is 39 (0x27). The field peak_duration_min_walking has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	s
Scaling	50
Default value	0.78
Range	Min=0.0, Max=5.10

- **peak_duration_min_running:** (bit offset: 8, bit width: 8, access: read-write) Minimum duration between two consecutive steps while running The reset value is 25 (0x19). The field peak_duration_min_running has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	s
Scaling	50
Default value	0.50
Range	Min=0.0, Max=5.10

Use this link to go back to the overview table: [STEP_COUNTER_9](#).

Register (0x2F) **STEP_COUNTER_10****Description:** Configuration for activity detection

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	0	1	1
Content	activity_detection_thres							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	0	0	1	1
Content	activity_detection_thres				activity_detection_factor			

- activity_detection_factor: (bit offset: 0, bit width: 4, access: read-write) Ratio of acceleration magnitude variance during running to walking The reset value is 3 (0x3).
- activity_detection_thres: (bit offset: 4, bit width: 12, access: read-write) Acceleration magnitude variance threshold for activity classification The reset value is 3900 (0xF3C). The field activity_detection_thres has the following properties:

Property	Value
Bitwidth	12
Sign	unsigned
Unit	g
Scaling	2048.0
Default value	3900/2048
Range	Min=0.0, Max=1.99951171875

Use this link to go back to the overview table: [STEP_COUNTER_10](#).

Register (0x30) **STEP_COUNTER_11****Description:** Configuration for time sparsity of step occurrence

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	0	0	0	0
Content	step_duration_window							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	0	1	1	0
Content	step_duration_max							

- **step_duration_max:** (bit offset: 0, bit width: 8, access: read-write) Maximum duration between two consecutive step occurrence The reset value is 150 (0x96). The field step_duration_max has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	s
Scaling	50
Default value	3
Range	Min=0.0, Max=5.10

- **step_duration_window:** (bit offset: 8, bit width: 8, access: read-write) Maximum duration since last step where next step shall be detected to add missed step, if any The reset value is 160 (0xA0). The field step_duration_window has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	s
Scaling	50
Default value	3.2
Range	Min=0.0, Max=5.10

Use this link to go back to the overview table: [STEP_COUNTER_11](#).

Register (0x31) **STEP_COUNTER_12****Description:** Configuration for post-processing of detected step for step count

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Content	reserved						mcr_thres	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	1	0	1	1	1
Content	mcr_thres			en_mcr_pp	step_dur_thres			en_step...

- reserved: do not interpret; in case of write, provide the reset value.
- en_step_dur_pp: (bit offset: 0, bit width: 1, access: read-write) Enable or disable post-processing for duration between steps
- step_dur_thres: (bit offset: 1, bit width: 3, access: read-write) Scale factor for mean step duration for step processing
The reset value is 3 (0x3). The field step_dur_thres has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Default value	3
Range	Min=0, Max=7

- en_mcr_pp: (bit offset: 4, bit width: 1, access: read-write) Enable or disable post-processing of step based on mean crossing
- mcr_thres: (bit offset: 5, bit width: 5, access: read-write) Threshold for number of mean crossings between two consecutive steps
The reset value is 14 (0xE). The field mcr_thres has the following properties:

Property	Value
Bitwidth	5
Sign	unsigned
Default value	14
Range	Min=0, Max=31

Use this link to go back to the overview table: [STEP_COUNTER_12](#).

Register (0x32) **STEP_COUNTER_13****Description:** Config parameter register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	0
Content	config_param_1							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	0	0	1	1
Content	config_param_1							

- config_param_1: (bit offset: 0, bit width: 16, access: read-write) config parameter 1 The reset value is 1219 (0x4C3).

Use this link to go back to the overview table: [STEP_COUNTER_13](#).

Register (0x33) **STEP_COUNTER_14****Description:** Config parameter register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	1
Content	config_param_2							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	1	0	1
Content	config_param_2							

- config_param_2: (bit offset: 0, bit width: 16, access: read-write) config parameter 2 The reset value is 2437 (0x985).

Use this link to go back to the overview table: [STEP_COUNTER_14](#).

Register (0x34) **STEP_COUNTER_15****Description:** Config parameter register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	0
Content	config_param_3							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	0	0	1	1
Content	config_param_3							

- config_param_3: (bit offset: 0, bit width: 16, access: read-write) config parameter 3 The reset value is 1219 (0x4C3).

Use this link to go back to the overview table: [STEP_COUNTER_15](#).

Register (0x35) **STEP_COUNTER_16**

Description: Config parameter register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	1	1	0
Content	config_param_4							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	1	1	0	0
Content	config_param_4							

- config_param_4: (bit offset: 0, bit width: 16, access: read-write) config parameter 4 The reset value is 59116 (0xE6EC).

Use this link to go back to the overview table: [STEP_COUNTER_16](#).

Register (0x36) **STEP_COUNTER_17**

Description: Config parameter register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	1	1	0
Content	config_param_5							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	1	1
Content	config_param_5							

- config_param_5: (bit offset: 0, bit width: 16, access: read-write) config parameter 5 The reset value is 17931 (0x460B).

Use this link to go back to the overview table: [STEP_COUNTER_17](#).

Register (0x37) **STEP_COUNTER_18**

Description: Config parameter register

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	0
Content	config_param_6							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	0
Content	config_param_6							

▪ config_param_6: (bit offset: 0, bit width: 16, access: read-write) config parameter 5 The reset value is 3598 (0xE0E).
Use this link to go back to the overview table: [STEP_COUNTER_18](#).

Register (0x38) **SIGNIFICANT_MOTION_1****Description:** Size of the segment for detection of significant motion

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	1	0	0
Content	segment_count						segment_size	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	0	0	1	0
Content	segment_size							

- segment_size: (bit offset: 0, bit width: 10, access: read-write) Size of the segment for detection of significant motion of the device. The reset value is 50 (0x32). The field segment_size has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	s
Scaling	50
Default value	1.0
Range	Min=0.0, Max=20.46

- segment_count: (bit offset: 10, bit width: 6, access: read-write) Number of segments to analyze for detection of significant motion of the device. When configured as 0, minimum segment count of 1 is assumed. The reset value is 5 (0x5). The field segment_count has the following properties:

Property	Value
Bitwidth	6
Sign	unsigned
Default value	5
Range	Min=0, Max=63

Use this link to go back to the overview table: [SIGNIFICANT_MOTION_1](#).

Register (0x39) **SIGNIFICANT_MOTION_2****Description:** Configuration of minimum value of peak to peak acceleration magnitude and mean crossing rate

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	1	0	0
Content	mcr_min						p2p_min	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	1	1	0
Content	p2p_min							

- **p2p_min:** (bit offset: 0, bit width: 10, access: read-write) Minimum value of the peak to peak acceleration magnitude
The reset value is 38 (0x26). The field p2p_min has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512
Default value	38/512
Range	Min=0.0, Max=1.998046875

- **mcr_min:** (bit offset: 10, bit width: 6, access: read-write) Minimum number of mean crossing per second in acceleration magnitude
The reset value is 17 (0x11). The field mcr_min has the following properties:

Property	Value
Bitwidth	6
Default value	17
Range	Min=0, Max=63

Use this link to go back to the overview table: [SIGNIFICANT_MOTION_2](#).

Register (0x3A) **SIGNIFICANT_MOTION_3**

Description: Configuration of maximum value of peak to peak acceleration magnitude and mean crossing rate

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	1	1	0
Content	mcr_max						p2p_max	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1	0	0	1	1
Content	p2p_max							

- **p2p_max:** (bit offset: 0, bit width: 10, access: read-write) Maximum value of the peak to peak acceleration magnitude
The reset value is 595 (0x253). The field p2p_max has the following properties:

Property	Value
Bitwidth	10
Sign	unsigned
Unit	g
Scaling	512
Default value	595/512
Range	Min=0.0, Max=1.998046875

- **mcr_max:** (bit offset: 10, bit width: 6, access: read-write) Maximum number of mean crossing per second in acceleration magnitude
The reset value is 17 (0x11). The field mcr_max has the following properties:

Property	Value
Bitwidth	6
Default value	17
Range	Min=0, Max=63

Use this link to go back to the overview table: [SIGNIFICANT_MOTION_3](#).

Register (0x3B) **WRIST_GESTURE_DETECTOR_1****Description:** Configuration for Setting 1

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	0
Content	min_flick_peak_y_threshold							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0
Content	min_flick_peak_y_threshold							

- min_flick_peak_y_threshold: (bit offset: 0, bit width: 16, access: read-write) Minimum flick peak threshold for Y axis The reset value is 1600 (0x640). The field min_flick_peak_y_threshold has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	g
Scaling	2048
Default value	0.78125
Range	Min=0.0, Max=31.99951171875

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_1](#).

Register (0x3C) **WRIST_GESTURE_DETECTOR_2****Description:** Configuration for Setting 2

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	min_flick_peak_z_threshold							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	1	1	1	0	0
Content	min_flick_peak_z_threshold							

- min_flick_peak_z_threshold: (bit offset: 0, bit width: 16, access: read-write) Minimum flick peak threshold for Z axis The reset value is 700 (0x2BC). The field min_flick_peak_z_threshold has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	g
Scaling	2048
Default value	0.341796875
Range	Min=0.0, Max=31.99951171875

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_2](#).

Register (0x3D) **WRIST_GESTURE_DETECTOR_3****Description:** Configuration for Setting 3

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	0	0
Content	gravity_bound_x_neg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	gravity_bound_x_neg							

- gravity_bound_x_neg: (bit offset: 0, bit width: 16, access: read-write) Gravity boundary limit for negative X axis The reset value is 64512 (0xFC00). The field gravity_bound_x_neg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048
Default value	0.5
Range	Min=0.0, Max=15.99951171875
Interpretation	sin(x)

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_3](#).

Register (0x3E) **WRIST_GESTURE_DETECTOR_4****Description:** Configuration for Setting 4

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1
Content	gravity_bound_x_pos							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	1	0	0
Content	gravity_bound_x_pos							

- gravity_bound_x_pos: (bit offset: 0, bit width: 16, access: read-write) Gravity boundary limit for positive X axis The reset value is 1924 (0x784). The field gravity_bound_x_pos has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048
Default value	0.939453125
Range	Min=0.0, Max=15.99951171875
Interpretation	sin(x)

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_4](#).

Register (0x3F) **WRIST_GESTURE_DETECTOR_5****Description:** Configuration for Setting 5

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	0	0
Content	gravity_bound_y_neg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	1	1	1
Content	gravity_bound_y_neg							

- gravity_bound_y_neg: (bit offset: 0, bit width: 16, access: read-write) Gravity boundary limit for negative Y axis The reset value is 64575 (0xFC3F). The field gravity_bound_y_neg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048
Default value	0.46923828125
Range	Min=0.0, Max=15.99951171875
Interpretation	sin(x)

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_5](#).

Register (0x40) **WRIST_GESTURE_DETECTOR_6****Description:** Configuration for Setting 6

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	0	0	1
Content	gravity_bound_z_neg							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	1	0
Content	gravity_bound_z_neg							

- gravity_bound_z_neg: (bit offset: 0, bit width: 16, access: read-write) Gravity boundary limit for negative Z axis The reset value is 63762 (0xF912). The field gravity_bound_z_neg has the following properties:

Property	Value
Bitwidth	16
Sign	signed
Unit	g
Scaling	2048
Default value	0.8662109375
Range	Min=0.0, Max=15.99951171875
Interpretation	cos(x)

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_6](#).

Register (0x43) **WRIST_GESTURE_DETECTOR_7****Description:** Configuration for Setting 7

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	max_duration_jiggle_peaks							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	0	0
Content	max_duration_jiggle_peaks							

- max_duration_jiggle_peaks: (bit offset: 0, bit width: 16, access: read-write) Maximum allowed time between two signal peaks to classify as jiggle gesture. The reset value is 16 (0x10). The field max_duration_jiggle_peaks has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	s
Scaling	50
Default value	0.32
Range	Min=0.0, Max=1310.7

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_7](#).

Register (0x44) **WRIST_GESTURE_DETECTOR_8****Description:** Configuration for Setting 8

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							device_...

- reserved: do not interpret; in case of write, provide the reset value.
- device_wear_position: (bit offset: 0, bit width: 1, access: read-write) Device wearing position
Following values can be set to or read from the field device_wear_position:

Value	Description
0b0 (0x0) (default)	Left arm / wrist
0b1 (0x1)	Right arm / wrist

Use this link to go back to the overview table: [WRIST_GESTURE_DETECTOR_8](#).

Register (0x45) **WRIST_WEAR_WAKEUP_1****Description:** Maximum tilt angle for focus pose in portrait direction

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	0	0	1
Content	angle_portrait_up							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	1	1	0
Content	angle_portrait_down							

- angle_portrait_down: (bit offset: 0, bit width: 8, access: read-write) Sine of the maximum allowed backward tilt angle in portrait down direction of the device, when it is in focus position (i.e. user is able to comfortably look at the dial of wear device). The reset value is 22 (0x16). The field angle_portrait_down has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	degrees
Scaling	256.0
Default value	4.9299
Range	Min=0, Max=44.3644
Interpretation	sin(angle)

- angle_portrait_up: (bit offset: 8, bit width: 8, access: read-write) Sine of the maximum allowed forward tilt angle in portrait up direction of the device, when it is in focus position (i.e. user is able to comfortably look at the dial of wear device) The reset value is 241 (0xF1). The field angle_portrait_up has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	degrees
Scaling	256.0
Default value	70.2891
Range	Min=60.1334, Max=74.7623
Interpretation	sin(angle)

Use this link to go back to the overview table: [WRIST_WEAR_WAKEUP_1](#).

Register (0x46) **WRIST_WEAR_WAKEUP_2****Description:** Maximum tilt angle for focus pose in landscape direction

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0
Content	angle_landscape_left							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0
Content	angle_landscape_right							

- **angle_landscape_right:** (bit offset: 0, bit width: 8, access: read-write) Sine of the maximum allowed tilt angle in landscape right direction of the device, when it is in focus position (i.e. user is able to comfortably look at the dial of wear device). The reset value is 128 (0x80). The field **angle_landscape_right** has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	degrees
Scaling	256.0
Default value	30
Range	Min=20, Max=30
Interpretation	sin(angle)

- **angle_landscape_left:** (bit offset: 8, bit width: 8, access: read-write) Sine of the maximum allowed tilt angle in landscape left direction of the device, when it is in focus position (i.e. user is able to comfortably look at the dial of wear device). The reset value is 128 (0x80). The field **angle_landscape_left** has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	degrees
Scaling	256.0
Default value	30
Range	Min=20, Max=30
Interpretation	sin(angle)

Use this link to go back to the overview table: [WRIST_WEAR_WAKEUP_2](#).

Register (0x47) **WRIST_WEAR_WAKEUP_3****Description:** Configuration for minimum change of orientation angle for gesture detection in non-focus pose

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	0
Content	min_angle_non_focus_pose							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	0	0	1
Content	min_angle_non_focus_pose							

- min_angle_non_focus_pose: (bit offset: 0, bit width: 16, access: read-write) Cosine of minimum expected angle change of the device when moving from non-focus to focus position The reset value is 1569 (0x621). The field min_angle_non_focus_pose has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	degrees
Scaling	2048.0
Default value	39.9939
Range	Min=25.0078, Max=45.0061
Interpretation	cos(angle)

Use this link to go back to the overview table: [WRIST_WEAR_WAKEUP_3](#).

Register (0x48) **WRIST_WEAR_WAKEUP_4****Description:** Configuration for minimum change of orientation angle for gesture detection in focus pose

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	0
Content	min_angle_focus_pose							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	1	0	0	1
Content	min_angle_focus_pose							

- min_angle_focus_pose: (bit offset: 0, bit width: 16, access: read-write) Cosine of minimum expected angle change of the device when moving within focus position. The reset value is 1737 (0x6C9). The field min_angle_focus_pose has the following properties:

Property	Value
Bitwidth	16
Sign	unsigned
Unit	degrees
Scaling	2048.0
Default value	31.9896
Range	Min=31.9896, Max=60
Interpretation	cos(angle)

Use this link to go back to the overview table: [WRIST_WEAR_WAKEUP_4](#).

Register (0x49) **WRIST_WEAR_WAKEUP_5****Description:** Configuration register for minimum durations in gesture classification

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	min_dur_static							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	min_dur_in_motion							

- **min_dur_in_motion:** (bit offset: 0, bit width: 8, access: read-write) Minimum duration the arm is expected to be in motion while a performing gesture The reset value is 2 (0x2). The field min_dur_in_motion has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	s
Scaling	50
Default value	0.04
Range	Min=0.0, Max=5.1

- **min_dur_static:** (bit offset: 8, bit width: 8, access: read-write) Minimum duration the device has to remain at a position to be considered as static The reset value is 2 (0x2). The field min_dur_static has the following properties:

Property	Value
Bitwidth	8
Sign	unsigned
Unit	s
Scaling	50
Default value	0.04
Range	Min=0.0, Max=5.1

Use this link to go back to the overview table: [WRIST_WEAR_WAKEUP_5](#).

Register (0x4A) **WRIST_WEAR_WAKEUP_6****Description:** Configuration for activation of wrist wear drop detection and stretch and pull down usecase

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						enable_...	enable_...

- reserved: do not interpret; in case of write, provide the reset value.
- enable_drop: (bit offset: 0, bit width: 1, access: read-write) Enable/disable wrist wear drop detection
Following values can be set to or read from the field enable_drop:

Value	Description
0b0 (0x0) (default)	Disable wrist wear drop detection position
0b1 (0x1)	Enable wrist wear drop detection position

- enable_arm_stretchpulldown: (bit offset: 1, bit width: 1, access: read-write) Enable/disable detection of stretch ad pull down use case
Following values can be set to or read from the field enable_arm_stretchpulldown:

Value	Description
0b0 (0x0) (default)	Disable detection of stretch ad pull down use case position
0b1 (0x1)	Enable detection of stretch ad pull down use case position

Use this link to go back to the overview table: [WRIST_WEAR_WAKEUP_6](#).

Register (0x4F) **VAD_1****Description:** Settings for voice activity detection

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R	R	R	R
Reset Value	0	0	0	1	0	1	0	0
Content	reserved			cls_mode	reserved			

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	1	0	1	0	1	1	1	1
Content	reserved					en_vad_chnl		

- reserved: do not interpret; in case of write, provide the reset value.
- en_vad_chnl: (bit offset: 0, bit width: 3, access: read-write) Selection of channel for detection of voice activity
Following values can be set to or read from the field en_vad_chnl:

Value	Description
0b000 (0x0)	Disable voice activity detection
0b001 (0x1)	Enable voice activity detection for channel x-only
0b010 (0x2)	Enable voice activity detection for channel y-only
0b011 (0x3)	Enable voice activity detection for channel x and y-only
0b100 (0x4)	Enable voice activity detection for channel z-only
0b101 (0x5)	Enable voice activity detection for channel x and z-only
0b110 (0x6)	Enable voice activity detection for channel y and z-only
0b111 (0x7) (default)	Enable voice activity detection for all channels

- cls_mode: (bit offset: 12, bit width: 1, access: read-write) Classification mode for voice activity
Following values can be set to or read from the field cls_mode:

Value	Description
0b0 (0x0)	Sensitive mode of voice detection
0b1 (0x1) (default)	Robust mode of voice detection

Use this link to go back to the overview table: [VAD_1](#).

Register (0x78) **ACC_ST****Description:** Configurations for the accelerometer self-test

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						sig_int_thres	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	1	0	0	1
Content	sig_int...	en_sig_...	samples_to_settle			samples_to_meas		

- reserved: do not interpret; in case of write, provide the reset value.
- samples_to_meas: (bit offset: 0, bit width: 3, access: read-write) Number of samples (at 1600 Hz) to measure for each polarity of BITE excitation. Number of samples = $4 \cdot 2^{\text{samples_to_meas}}$. The reset value is 1 (0x1).
- samples_to_settle: (bit offset: 3, bit width: 3, access: read-write) Number of samples to wait before measuring data during accel self test, Wait-Time in s = $(2^{\text{samples_to_settle}}) / 1600\text{Hz}$. The reset value is 3 (0x3).
- en_sig_int_valid: (bit offset: 6, bit width: 1, access: read-write) Enable signal integrity check after accelerometer self-test.
- sig_int_thres: (bit offset: 7, bit width: 3, access: read-write) Threshold for signal integrity check after accelerometer self-test. Range = 0 to 7. Value = $(0.0034 + 0.004 \cdot x^2)$ g. The reset value is 1 (0x1). The field sig_int_thres has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	g
Default value	0.0074
Range	Min=0.0034, Max=0.1994

Use this link to go back to the overview table: [ACC_ST](#).

Register (0x7D) **ACC_OFFSETS_EST_1****Description:** Accelerometer offset error estimation configurations

Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	axis_1g			reserved	apply_corr	reserved	sig_int_thres	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	0	0	1	1
Content	sig_int...	en_sig...	samples_to_settle			samples_to_measure		

- reserved: do not interpret; in case of write, provide the reset value.
- samples_to_measure: (bit offset: 0, bit width: 3, access: read-write) Number of 50Hz accelerometer samples that are averaged to estimate the offset. Number of samples = $2^{\text{samples_to_measure}}$. The reset value is 3 (0x3).
- samples_to_settle: (bit offset: 3, bit width: 3, access: read-write) Number of samples to wait before measuring data during accel offset error estimation. Wait-Time in s = $(2^{\text{samples_to_settle}}) / 50\text{Hz}$. The reset value is 2 (0x2).
- en_sig_int_valid: (bit offset: 6, bit width: 1, access: read-write) Enable signal integrity check for accelerometer offset error estimation.
- sig_int_thres: (bit offset: 7, bit width: 3, access: read-write) Threshold for signal integrity check after accelerometer offset error estimation. Range = 0 to 7. Value = $(0.001 + 0.004 \cdot x^2)$ g The reset value is 1 (0x1). The field sig_int_thres has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	g
Default value	0.005
Range	Min=0.001, Max=0.197

- apply_corr: (bit offset: 11, bit width: 1, access: read-write) Update user offset registers with estimated offset values after feature completion
- axis_1g: (bit offset: 13, bit width: 3, access: read-write) Accelerometer offset error estimation must only be executed when the device is still and one axis is parallel to the gravitation vector. This axis can be either aligned with gravitational vector or in the opposite direction of the gravitational vector. Device will not warn the user if the device is not static or an axis is not parallel to the gravitational vector.

Following values can be set to or read from the field axis_1g:

Value	Description
0b000 (0x0) (default)	Z-axis shows 1G
0b001 (0x1)	Z-axis shows -1G
0b010 (0x2)	Y-axis shows 1G
0b011 (0x3)	Y-axis shows -1G
0b100 (0x4)	X-axis shows 1G
0b101 (0x5)	X-axis shows -1G

Use this link to go back to the overview table: [ACC_OFFSETS_EST_1](#).

Register (0x7E) **GYR_ST_CONF_1****Description:** Configuration register 1 for the gyroscope self-test

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	reserved						sig_int_thres	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	0	0	1	1
Content	sig_int...	en_sig_...	samples_to_settle			samples_to_measure		

- reserved: do not interpret; in case of write, provide the reset value.
- samples_to_measure: (bit offset: 0, bit width: 3, access: read-write) Number of gyroscope samples averaged (at ~171Hz) during gyroscope self-test for one polarity = $8 \cdot 2^{\text{samples_to_measure}}$. For the recommended value, refer to the functional description section. The reset value is 3 (0x3). The field samples_to_measure has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Default value	64
Range	Min=8, Max=1024

- samples_to_settle: (bit offset: 3, bit width: 3, access: read-write) Number of samples to wait before measuring data during gyroscope self-test. Wait-Time in s = $(2^{\text{samples_to_settle}}) / \sim 171\text{Hz}$. For the recommended value, refer to the functional description section. The reset value is 4 (0x4).
- en_sig_int_valid: (bit offset: 6, bit width: 1, access: read-write) Enable signal integrity check for gyroscope self-test.
- sig_int_thres: (bit offset: 7, bit width: 3, access: read-write) Threshold for signal integrity check after gyroscope self-test. Range = 0 to 7. Value = $(0.125 + 0.2015 \cdot x^2)$ dps. The reset value is 1 (0x1). The field sig_int_thres has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	dps
Default value	0.3265
Range	Min=0.125, Max=9.9985

Use this link to go back to the overview table: [GYR_ST_CONF_1](#).

Register (0x7F) **GYR_ST_CONF_2****Description:** Configuration register 2 for the gyroscope self-test

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	0	1	0
Content	reserved		motion_detect_thres					en_moti...

- reserved: do not interpret; in case of write, provide the reset value.
- en_motion_detect: (bit offset: 0, bit width: 1, access: read-write) Enable accelerometer based motion detection during gyroscope self-test.
- motion_detect_thres: (bit offset: 1, bit width: 5, access: read-write) Maximum acceptable acceleration change between two accelerometer samples. Range = 0 to 31. Value = $3\text{mg} + 0.6212 * \text{thres}^2$. The reset value is 13 (0xD). The field motion_detect_thres has the following properties:

Property	Value
Bitwidth	5
Sign	unsigned
Unit	mg
Default value	108
Range	Min=3.0, Max=600.0

Use this link to go back to the overview table: [GYR_ST_CONF_2](#).

Register (0x81) **GYR_OFFS_EST_1****Description:** Gyroscope offset error estimation configurations

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R	R/W	R/W
Reset Value	0	0	0	0	1	0	0	1
Content	reserved				apply_corr	reserved	sig_int_thres	

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	0	1	0
Content	sig_int...	en_sig_...	samples_to_settle			samples_to_measure		

- reserved: do not interpret; in case of write, provide the reset value.
- samples_to_measure: (bit offset: 0, bit width: 3, access: read-write) Number of gyroscope samples (at 1600 Hz) averaged during gyroscope offset error estimation = $64 \cdot 2^{\text{samples_to_measure}}$. The reset value is 2 (0x2). The field samples_to_measure has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Default value	256
Range	Min=64, Max=8192

- samples_to_settle: (bit offset: 3, bit width: 3, access: read-write) Number of samples to wait before measuring data during gyroscope offset error estimation. Wait-Time in s = $(2^{\text{samples_to_settle}}) / 1600\text{Hz}$. The reset value is 4 (0x4).
- en_sig_int_valid: (bit offset: 6, bit width: 1, access: read-write) Enable signal integrity check for gyroscope offset error estimation.
- sig_int_thres: (bit offset: 7, bit width: 3, access: read-write) Threshold for signal integrity check after gyroscope offset error estimation. Range = 0 to 7. Value = $(0.184 + 0.2 \cdot x^2)$ dps The reset value is 2 (0x2). The field sig_int_thres has the following properties:

Property	Value
Bitwidth	3
Sign	unsigned
Unit	dps
Default value	0.9840
Range	Min=0.184, Max=9.9840

- apply_corr: (bit offset: 11, bit width: 1, access: read-write) Update user offset registers with estimated offset values after feature completion

Use this link to go back to the overview table: [GYR_OFFS_EST_1](#).

Register (0x82) **GYR_OFFS_EST_2****Description:** Gyroscope offset error estimation configurations

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	0	1	0
Content	reserved		motion_detect_thres					en_moti...

- reserved: do not interpret; in case of write, provide the reset value.
- en_motion_detect: (bit offset: 0, bit width: 1, access: read-write) Enable accelerometer based motion detection during gyroscope offset error estimation.
- motion_detect_thres: (bit offset: 1, bit width: 5, access: read-write) Maximum acceptable acceleration change between two accelerometer samples. Range = 0 to 31. Value = $3\text{mg} + 0.6212 * \text{thres}^2$. The reset value is 13 (0xD). The field motion_detect_thres has the following properties:

Property	Value
Bitwidth	5
Sign	unsigned
Unit	mg
Default value	108
Range	Min=3.0, Max=600.0

Use this link to go back to the overview table: [GYR_OFFS_EST_2](#).

Register (0x8F) **ST_RESULT****Description:** Self-test (accelerometer and gyroscope) results

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							gyr_st_ok

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_st_ok	gyr_dri...	gyr_sen...	gyr_sen...	gyr_sen...	acc_sen...	acc_sen...	acc_sen...

- reserved: do not interpret; in case of write, provide the reset value.
- acc_sens_x_ok: (bit offset: 0, bit width: 1, access: read-write) Self-test result of accelerometer X-axis
Following values can be set to or read from the field acc_sens_x_ok:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- acc_sens_y_ok: (bit offset: 1, bit width: 1, access: read-write) Self-test result of accelerometer Y-axis
Following values can be set to or read from the field acc_sens_y_ok:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- acc_sens_z_ok: (bit offset: 2, bit width: 1, access: read-write) Self-test result of accelerometer Z-axis
Following values can be set to or read from the field acc_sens_z_ok:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- gyr_sens_x_ok: (bit offset: 3, bit width: 1, access: read-write) Self-test result of gyroscope X-axis
Following values can be set to or read from the field gyr_sens_x_ok:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- gyr_sens_y_ok: (bit offset: 4, bit width: 1, access: read-write) Self-test result of gyroscope Y-axis
Following values can be set to or read from the field gyr_sens_y_ok:

Value	Description
-------	-------------

0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- **gyr_sens_z_ok:** (bit offset: 5, bit width: 1, access: read-write) Self-test result of gyroscope Z-axis
Following values can be set to or read from the field **gyr_sens_z_ok**:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- **gyr_drive_ok:** (bit offset: 6, bit width: 1, access: read-write) Self-test result of gyroscope drive
Following values can be set to or read from the field **gyr_drive_ok**:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- **acc_st_ok:** (bit offset: 7, bit width: 1, access: read-write) Self-test of accelerometer successful
Following values can be set to or read from the field **acc_st_ok**:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

- **gyr_st_ok:** (bit offset: 8, bit width: 1, access: read-write) Self-test of gyroscope successful
Following values can be set to or read from the field **gyr_st_ok**:

Value	Description
0b1 (0x1)	Self-test succeeded
0b0 (0x0) (default)	Self-test failed

Use this link to go back to the overview table: [ST_RESULT](#).

Register (0x90) **ACC_OFFSETS_EST_8G_X****Description:** Accelerometer offset estimation result for 8g range X-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_8g_x							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_8g_x: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for accelerometer X-axis in 8g range. The reset value is 0 (0x0). The field offs_est_8g_x has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	mg
Scaling	1.953125
Default value	0
Range	Min=-250.0, Max=248.046875

Use this link to go back to the overview table: [ACC_OFFSETS_EST_8G_X](#).

Register (0x91) **ACC_OFFSETS_EST_8G_Y**

Description: Accelerometer offset estimation result for 8g range Y-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_8g_y							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_8g_y: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for accelerometer Y-axis in 8g range. The reset value is 0 (0x0). The field offs_est_8g_y has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	mg
Scaling	1.953125
Default value	0
Range	Min=-250.0, Max=248.046875

Use this link to go back to the overview table: [ACC_OFFSETS_EST_8G_Y](#).

Register (0x92) **ACC_OFFSETS_EST_8G_Z****Description:** Accelerometer offset estimation result for 8g range Y-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_8g_z							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_8g_z: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for accelerometer Y-axis in 8g range. The reset value is 0 (0x0). The field offs_est_8g_z has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	mg
Scaling	1.953125
Default value	0
Range	Min=-250.0, Max=248.046875

Use this link to go back to the overview table: [ACC_OFFSETS_EST_8G_Z](#).

Register (0x93) **ACC_OFFSETS_EST_32G_X****Description:** Accelerometer offset estimation result for 32g range X-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_32g_x							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_32g_x: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for accelerometer X-axis in 32g range. The reset value is 0 (0x0). The field offs_est_32g_x has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	mg
Scaling	7.8125
Default value	0
Range	Min=-1000.0, Max=992.1875

Use this link to go back to the overview table: [ACC_OFFSETS_EST_32G_X](#).

Register (0x94) **ACC_OFFSETS_EST_32G_Y****Description:** Accelerometer offset estimation result for 32g range Y-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_32g_y							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_32g_y: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for accelerometer Y-axis in 32g range. The reset value is 0 (0x0). The field offs_est_32g_y has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	mg
Scaling	7.8125
Default value	0
Range	Min=-1000.0, Max=992.1875

Use this link to go back to the overview table: [ACC_OFFSETS_EST_32G_Y](#).

Register (0x95) **ACC_OFFSETS_EST_32G_Z**

Description: Accelerometer offset estimation result for 32g range Y-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_32g_z							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_32g_z: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for accelerometer Y-axis in 32g range. The reset value is 0 (0x0). The field offs_est_32g_z has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	mg
Scaling	7.8125
Default value	0
Range	Min=-1000.0, Max=992.1875

Use this link to go back to the overview table: [ACC_OFFSETS_EST_32G_Z](#).

Register (0x96) **GYR_OFFS_EST_X****Description:** Gyroscope offset estimation result for X-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_x							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_x: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for gyroscope X-Axis The reset value is 0 (0x0). The field offs_est_x has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	dps
Scaling	0.1220703125
Range	Min=-15.625, Max=15.5029296875

Use this link to go back to the overview table: [GYR_OFFS_EST_X](#).

Register (0x97) **GYR_OFFS_EST_Y****Description:** Gyroscope offset estimation result for Y-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_y							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_y: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for gyroscope Y-Axis The reset value is 0 (0x0). The field offs_est_y has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	dps
Scaling	0.1220703125
Range	Min=-15.625, Max=15.5029296875

Use this link to go back to the overview table: [GYR_OFFS_EST_Y](#).

Register (0x98) **GYR_OFFS_EST_Z****Description:** Gyroscope offset estimation result for Z-Axis

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	offs_est_z							

- reserved: do not interpret; in case of write, provide the reset value.
- offs_est_z: (bit offset: 0, bit width: 8, access: read-write) Offset error estimated for gyroscope Z-Axis The reset value is 0 (0x0). The field offs_est_z has the following properties:

Property	Value
Bitwidth	8
Sign	signed
Unit	dps
Scaling	0.1220703125
Range	Min=-15.625, Max=15.5029296875

Use this link to go back to the overview table: [GYR_OFFS_EST_Z](#).

Register (0x9D) **AXIS_MAP****Description:** Describes axis map settings

Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		invert_z	invert_y	invert_x	axis_ex		

- reserved: do not interpret; in case of write, provide the reset value.
- axis_ex: (bit offset: 0, bit width: 3, access: read-write) Map accelerometer and gyroscope axis to desired axis exchange in the form new_axis=old_axis
Following values can be set to or read from the field axis_ex:

Value	Description
0b000 (0x0) (default)	x_new=x_old; y_new=y_old; z_new=z_old;
0b001 (0x1)	x_new=y_old; y_new=x_old; z_new=z_old;
0b010 (0x2)	x_new=x_old; y_new=z_old; z_new=y_old;
0b011 (0x3)	x_new=z_old; y_new=x_old; z_new=y_old;
0b100 (0x4)	x_new=y_old; y_new=z_old; z_new=x_old;
0b101 (0x5)	x_new=z_old; y_new=y_old; z_new=x_old;
0b110 (0x6)	same as 0
0b111 (0x7)	same as 0

- invert_x: (bit offset: 3, bit width: 1, access: read-write) Invert the x axis of accelerometer and gyroscope
Following values can be set to or read from the field invert_x:

Value	Description
0b0 (0x0) (default)	Clear this bit to not invert the sign of the x axis
0b1 (0x1)	Set this bit to invert the sign of the x axis

- invert_y: (bit offset: 4, bit width: 1, access: read-write) Invert the y axis of accelerometer and gyroscope
Following values can be set to or read from the field invert_y:

Value	Description
0b0 (0x0) (default)	Clear this bit to not invert the sign of the y axis
0b1 (0x1)	Set this bit to invert the sign of the y axis

- invert_z: (bit offset: 5, bit width: 1, access: read-write) Invert the z axis of accelerometer and gyroscope
Following values can be set to or read from the field invert_z:

Value	Description
-------	-------------

0b0 (0x0) (default)	Clear this bit to not invert the sign of the z axis
0b1 (0x1)	Set this bit to invert the sign of the z axis

Use this link to go back to the overview table: [AXIS_MAP](#).

8 Pin Out and Connection Diagrams

8.1 Pin Out

Figures 33 and 34 show the pin-out of the device from top and bottom view, respectively.

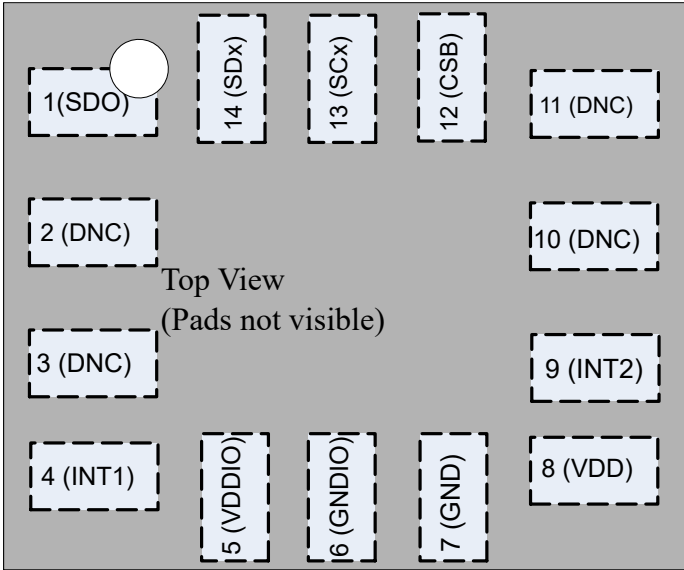


Figure 33: Pin Out Top View

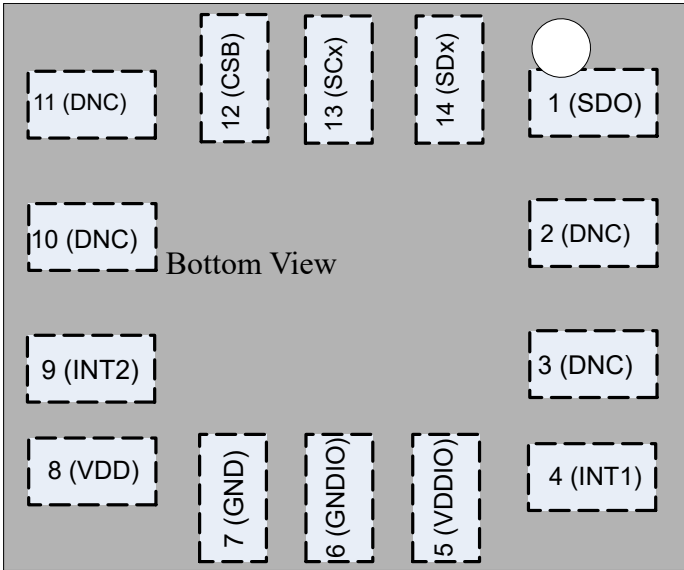


Figure 34: Pin Out Bottom View

Table 59 details the pin out and the electrical communication connections possible with the individual pins of the device. The following abbreviations are used in the pin descriptions: NC means “not connected” and DNC means “do not connect”.

Table 59: Pin-out and pin connections

Pin	Name	I/O Type	I/F	Description	Connect to		
#					in SPI 4w	in SPI 3w	in I ² C/I ³ C
1	SDO	Digital I/O	Prim.	SDO Serial data output in SPI 4W	SDO	DNC	GND for default I ² C address VDDIO for alternative I ² C address
				I ² C / I ³ C Address bit-0 (selection during boot)			
2	NC				DNC or VDDIO		
3	NC				DNC or VDDIO		
4	INT1	Digital I/O		Interrupt Pin 1	if used INT1, otherwise DNC		
5	VDDIO	Supply		Digital I/O supply voltage 1.08V ...3.63V	VDDIO		
6	GNDIO	Ground		Ground for I/O	GNDIO		
7	GND	Ground		Ground for digital & analog	GND		
8	VDD	Supply		Power supply analog & digital domain 1.71V ...3.63V	VDD		
9	INT2	Digital I/O		Interrupt pin 2	if used INT2, otherwise DNC		
10	NC				DNC or VDDIO		
11	NC				DNC or VDDIO		
12	CSB	Digital I/O	Prim.	Chip select for SPI mode	CSB		VDDIO
13	SCx	Digital I/O	Prim.	SPI: SCK for serial clock	SCK	SCK	SCL
				I ² C/I ³ C: SCL for serial clock			
14	SDx	Digital I/O	Prim.	SDA serial data I/O in I ² C/I ³ C	SDI	SDX	SDA
				SDI serial data input in SPI 4-wire			
				SDA serial data I/O in SPI 3-wire			

8.2 Connection Diagrams

It is recommended to use 100 nF capacitors for decoupling at pin 5 (VDDIO) and pin 8 (VDD).

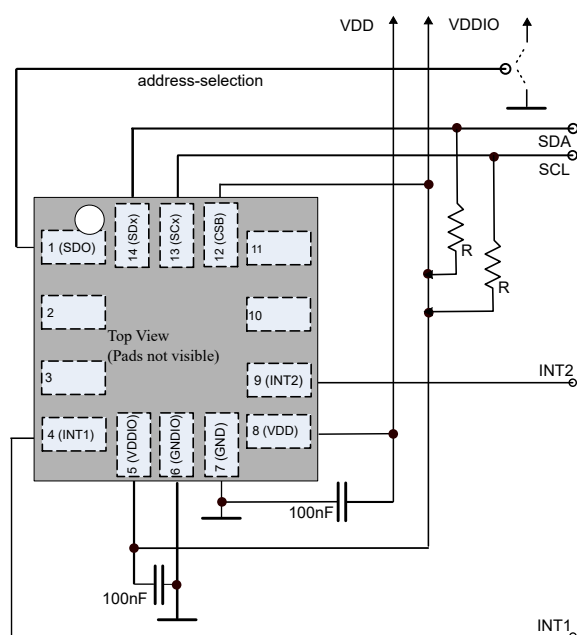
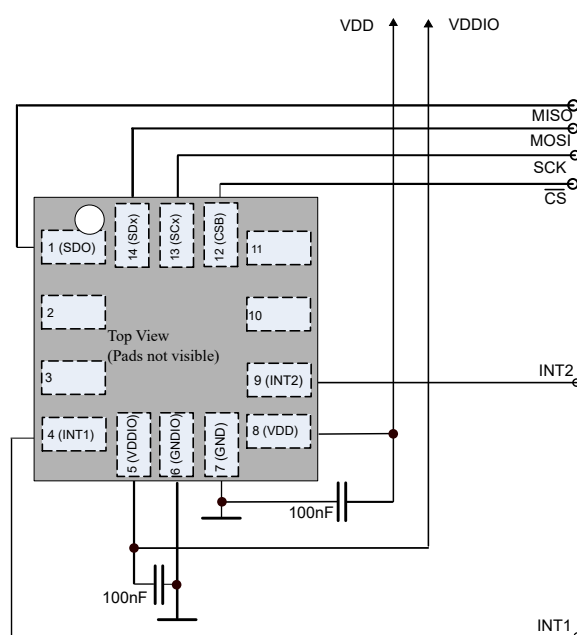
Figure 35: Pin connection with I²C/I3C

Figure 36: Pin connection with SPI 4-wire

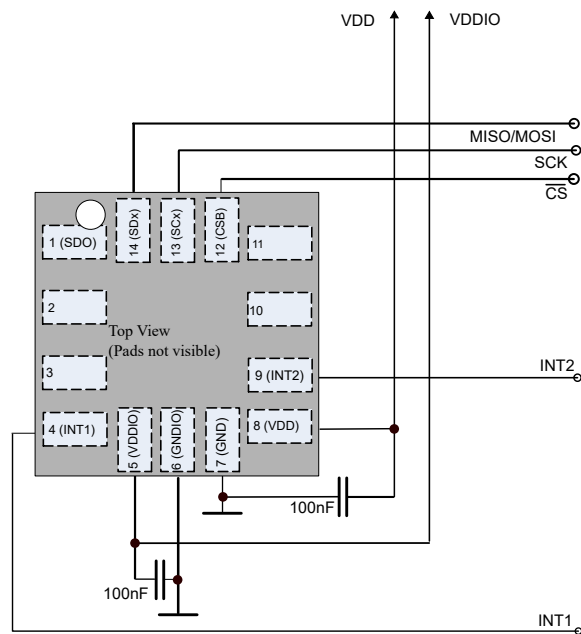


Figure 37: Pin connection with SPI 3-wire

9 Package

9.1 Dimensions

The Figures 38, 39 and 40 depict the dimensions of the package. The dimensions D, E and F for the package outline and the dimensions L, L1 and b for the pads are stated in Table 60.

Table 60: Basic mechanical parameter specification

Parameter	Symbol	Condition	Min	Typ	Max	Units
Length	D	–	2.95	3.00	3.05	mm
Width	E	–	2.45	2.50	2.55	mm
Height	F	–	0.78	0.83	0.88	mm
Pad length	L	–	0.425	0.475	0.525	mm
Pad width	b	–	0.20	0.25	0.30	mm
Distance between pads	e	Basic spacing between centers		0.50		mm
Distance between outer pads on long side	D1	Basic spacing between centers		1.00		mm
Distance between outer pads on wide side	E1	Basic spacing between centers		1.50		mm
Distance package to pad	L1	–	0.05	0.10	0.15	mm

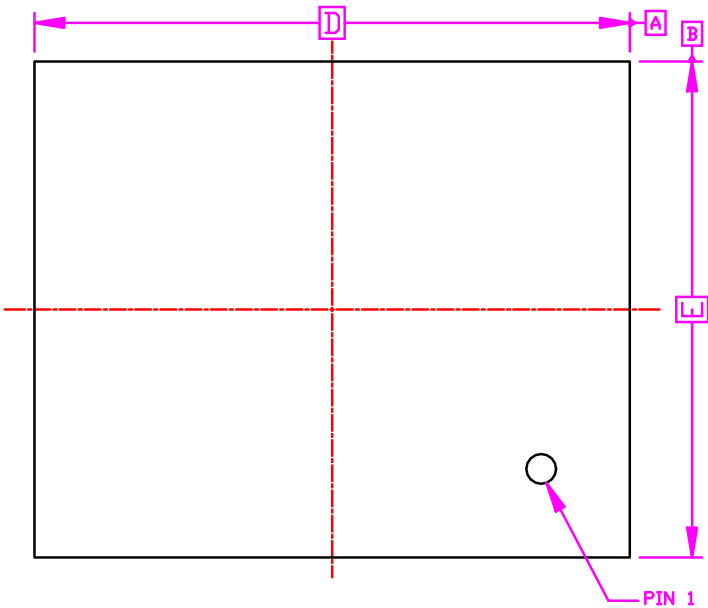


Figure 38: Dimensions from top view

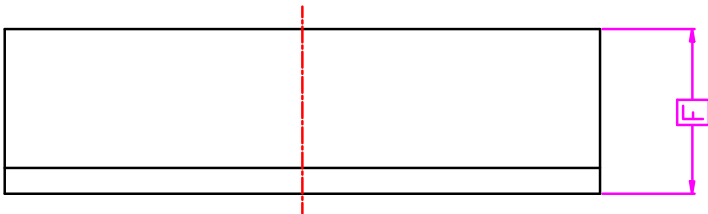


Figure 39: Dimensions from side view

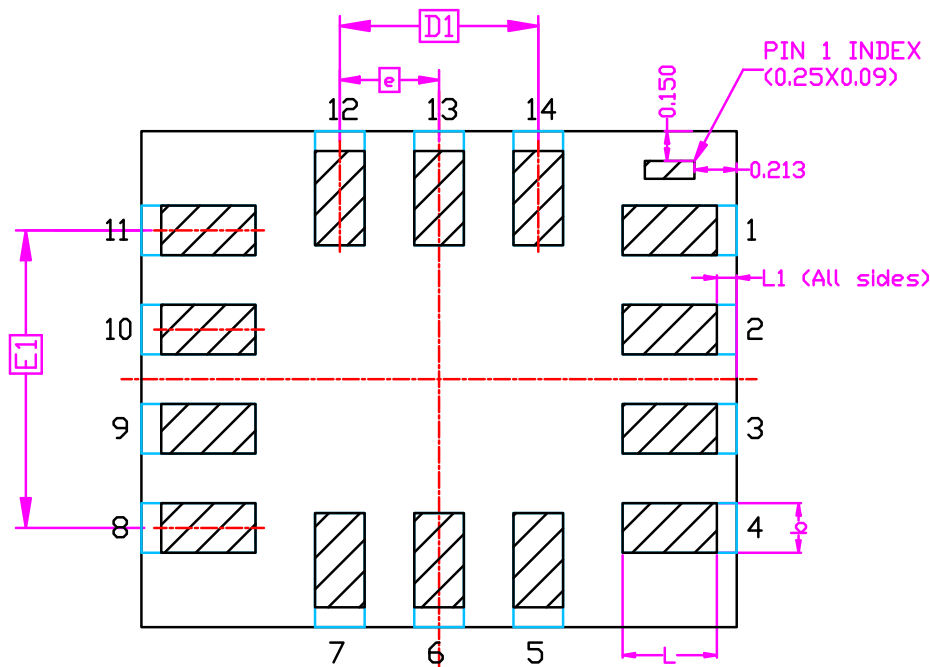


Figure 40: Dimensions from bottom view

9.2 Sensing Axes Orientation

If the sensor is accelerated and/or rotated in the indicated directions, the corresponding channels of the device will deliver a positive acceleration and/or yaw rate signal (dynamic acceleration). If the sensor is at rest without any rotation and the force of gravity is acting contrary to the indicated directions, the output of the corresponding acceleration channel will be positive and the corresponding gyroscope channel will be “zero” (static acceleration).

Example: if the sensor is at rest or at uniform motion in a gravity field according to the figure given below, the output signals are:

- $\pm 0g$ for the a_x accelerometer channel and $\pm 0^\circ/s$ for the Ω_x gyroscope channel
- $\pm 0g$ for the a_y accelerometer channel and $\pm 0^\circ/s$ for the Ω_y gyroscope channel
- $+1g$ for the a_z accelerometer channel and $\pm 0^\circ/s$ for the Ω_z gyroscope channel

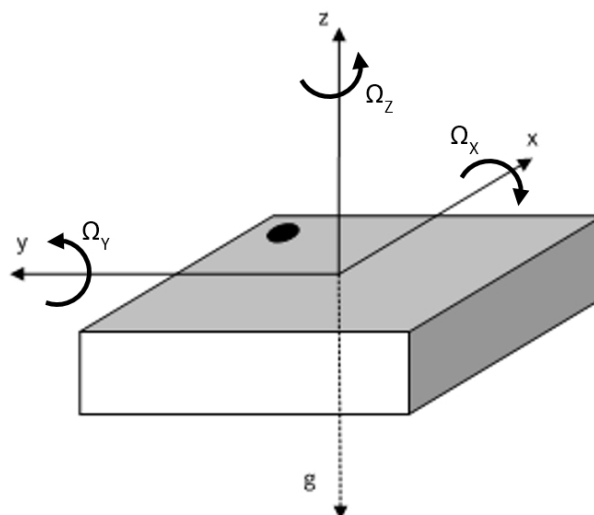
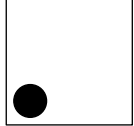
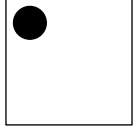
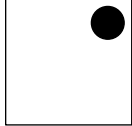
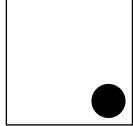


Figure 41: Definition of the sensing axes orientation for the raw device

For reference, Figure 42 below shows the smartphone device orientation with an integrated device.

Table 61: Output value corresponding to device orientation

Sensor Orientation (gravity vector ↓)					upright	upside down
Output Signal X	0 g / 0 LSB	+1 g / +1048576 LSB	0 g / 0 LSB	-1 g / -1048576 LSB	0 g / 0 LSB	0 g / 0 LSB
Output Signal Y	-1 g / -1048576 LSB	0 g / 0 LSB	+1 g / +1048576 LSB	0 g / 0 LSB	0 g / 0 LSB	0 g / 0 LSB
Output Signal Z	0 g / 0 LSB	0 g / 0 LSB	0 g / 0 LSB	0 g / 0 LSB	+1 g / +1048576 LSB	-1 g / -1048576 LSB

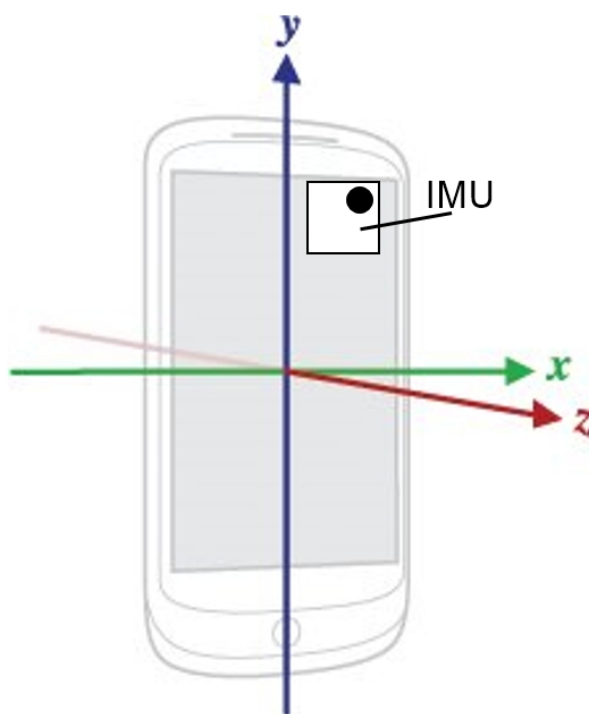


Figure 42: Definition of the sensing axes orientation within a device

Table 61 lists all corresponding output signals on X, Y, and Z of an ideal sensor¹ at rest or at uniform motion in a gravity field. For the output an $\pm 8g$ range setting, 24 bit resolution, and a top down gravity vector, as indicated in the top left most cell, are assumed.

If the sensor axes coordinates do not match the axes coordinates of the platform, then a remapping of the axes is required. For the accelerometer and gyroscope data, the axes remapping may be done by the sensor internal axes remapping feature, see section 5.11.2, or may be implemented in the driver of the application processor. To ensure the expected function of the advanced features according to the desired coordinate system, the sensor internal remapping of the axes is needed.

9.3 Soldering Landing Pattern

Figure 43 provides the recommendation for the positioning of the landing of the soldering pads to ensure maximum stability of the solder connections.

¹For demonstration purposes possible sensitivity or offset errors are neglected.

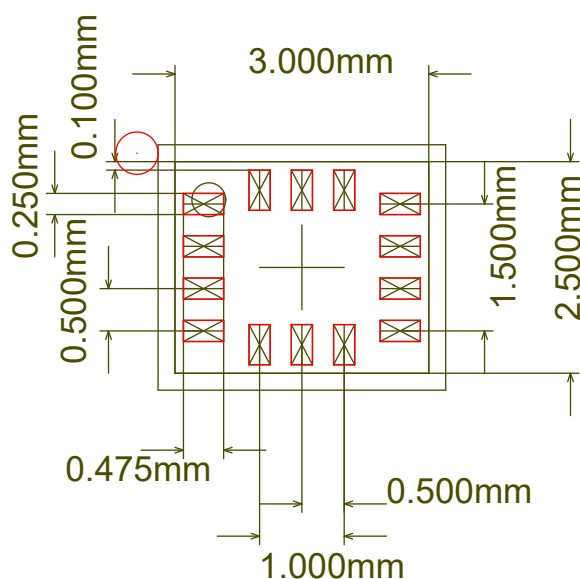


Figure 43: Recommended PCB landing pattern

9.4 Marking

Mass Production

Labeling	Symbol	Name	Remark
● P N C C C	P	Product Identifier	
	N	Internal Code	
	CCC	Counter ID	
	•	Pin 1	Identifier on top side

Engineering Samples

Labeling	Symbol	Name	Remark
● N E C C C	N	Product Identifier	
	E	Internal Code	
	CCC	Counter ID	
	•	Pin 1	Identifier on top side

9.5 Tape and Reel Information

The tape and reel information for BMI423 is available within the document “Handling, Soldering, and Mounting Instructions” (HSMI). This document can be retrieved from the BST homepage.

9.6 Soldering Guidelines

The moisture sensitivity level of the device corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020E “Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices”
- IPC/JEDEC J-STD-033D “Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices”

Both documents are available on the JEDEC website <https://www.jedec.org/>.

The sensor fulfills the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, that means reflow soldering with a peak temperature $T_{\text{solder,pk}}$ up to 260°C.

9.7 Handling Instructions

Micromechanical sensors are designed to sense acceleration with high accuracy even at low amplitudes and contain highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand *g*. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping of the sensor onto hard surfaces etc.

We recommend to avoid accelerations beyond the specified limits during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (e.g. 2kV HBM); however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

For more details on recommended handling, soldering and mounting please refer to the corresponding “Handling, soldering and mounting instructions” document or contact our regional offices, distributors and sales representatives.

9.8 Environmental Safety

This device complies with directive 2011/65/EU (RoHS) and its subsequent amendments, restricting the use of hazardous substances in electrical and electronic equipment. This device complies with the industry standard IEC 61249. For more details on the corresponding analysis results, please contact your Bosch Sensortec representative.

10 Legal disclaimer

10.1 Engineering samples

Engineering Samples are marked with an asterisk (*), (E), (e), (F), (A) or (C) or have 2DID code. In case of 2DID Code, a sample identifier is specified in the Laser marking section in the product data sheet. Samples may vary from the valid technical specifications of the product series contained in this data sheet. They are therefore not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a product series. Bosch Sensortec assumes no liability for the use of engineering samples. The purchaser or the recipient of Engineering Samples shall indemnify Bosch Sensortec from all claims arising from the use of engineering samples.

10.2 Product use

Bosch Sensortec products are developed for the consumer goods industry. They may only be used within the parameters of this product data sheet. They are not fit for use in life-sustaining or safety-critical systems. Safety-critical systems are those for which a malfunction is expected to lead to bodily harm, death or severe property damage. In addition, they shall not be used directly or indirectly for military purposes (including but not limited to nuclear, chemical or biological proliferation of weapons or development of missile technology), nuclear power, deep sea or air or space applications (including but not limited to satellite technology) or supercomputers. If the purchaser would like to use Bosch Sensortec products in supercomputers, the purchaser is obligated to get prior written explicit permissions from Bosch Sensortec.

Bosch Sensortec products are released on the basis of the legal and normative requirements relevant to the Bosch Sensortec product for use in the following geographical target market: BE, BG, CZ, DK, DE, EE, IE, EL, ES, FR, HR, IT, CY, LV, LT, LU, HU, MT, NL, AT, PL, PT, RO, SI, SK, FI, SE, US, CN, JP, KR, TW, AU, CA, CH, GB, IL, IN, MY, SG, TH, TN, VN. If the purchaser needs further information or has further requirements, please contact the local sales contact.

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The purchaser shall indemnify Bosch Sensortec from all third party claims arising from any product use not covered by the parameters of this product data sheet or not approved by Bosch Sensortec and reimburse Bosch Sensortec for all costs in connection with such claims.

The purchaser accepts the responsibility to monitor the market for the purchased products, particularly with regard to product safety, and to inform Bosch Sensortec without delay of all safety-critical incidents.

10.3 Application examples and hints

With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Bosch Sensortec hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights or copyrights of any third party. The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. They are provided for illustrative purposes only and no evaluation regarding infringement of intellectual property rights or copyrights or regarding functionality, performance or error has been made.

11 Document History and Modifications

Table 62: Change Log

Rev No	Chapter	Description of modification/changes	Date
1.0		Product release	Oct 9th 2026

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